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IMPLEMENTATION OF HIGH PERFORMANCE PROCESSOR ON DE-10 LITE MAX10 INTEL ALTERAFPGA

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***Abstract*— Nowadays application specific soft processor cores are gaining importance for FPGA based embedded applications in which user can configure the processor as per requirement. The architecture of high performance processor that is implemented is a RISC soft-core architecture which is implemented entirely in the programmable logic and memory blocks of Altera FPGAs. The architectural simplicity of RISC processors makes the suitable for low power applications. The soft-core nature of this processorlets the system designer specify and generate a custom processor core, tailored for his or her specific application requirements. System designers can extend the basic functionality of this processor by adding a predefined memory management unit, or defining custom instructions and custom peripherals which is also shown in this project. As a part of the project that is proposed in thispaper we will design the hardware that creates the high performance NIOS II soft processor using Qsys (Platform Builder) with several interfaces to devices on the DE10-Lite and develop software for the same using several interfaces to devices on the DE10-Lite development kit.**

***Index Terms*— Altera FPGA, High Performance Processor, MAX10 DE10-Lite, NIOS II soft processor, Qsys**

I. INTRODUCTION

The most common embedded software implementation involves the mapping of soft core processors onto field-programmable gate arrays (FPGAs). Soft core microprocessors serves to be the best solution as they have a re-configurable architecture and custom hardware / logic can be easily interfaced to the processor. Field-Programmable gate array (FPGA) vendors now support processors on their FPGA devices to allow complete systems to be implemented on a single programmable chip. The soft-core processors are fully described using hardware description language (HDL). They can be synthesized for any Application-Specific Integrated Circuit (ASIC) or Field Programmable Gate Array (FPGA) technology.

With a standard chip, such as the Intel Curie module in an Arduino board or a CPU in your laptop, the chip is fully baked. It can't be programmed; you get what you get. With these chips, a user can write software that loads onto a chip and executes functions. That software can later be replaced or deleted, but the hardware chip remains unchanged. With an FPGA, there is no chip. The user programs the hardware circuit or circuits. The programming can be a single, simple logic gate (an AND or OR function), or it can involve one or more complex functions, including functions that, together, act as a comprehensive multi-core processor.

The 'NIOS II,' soft-core processor is used in the proposed system design. The 'NIOS II,' soft-core processor is a general-purpose 16/32-bit RISC processor that can be implemented on 'ALTERA' programmable logic devices (PLD). Intel Altera DE-10 Lite FPGA kit is used for implementation

II. DESIGN OF A SYSTEM USING NIOS IIPROCESSOR

We will create a design in Qsys, the Altera System Design Tool, which includes a NIOS II softcore CPU, On-chip RAM and FLASH memory for program and data storage, a 1 ms System Timer, System ID block, MAX10 ADC module, LED and slide switch interfaces, SDRAM controller, SPI bus interface to an accelerometer, and JTAG connections to the software development and FPGA configuration tools, all connected together by a Avalon Bus or Bus Bridge. The inputs are a System Clock at 50 MHz, a 10 MHz ADC clock, 10 slide switch inputs, SPI data from the accelerometer, and the ADC input from a pin on the Arduino Analog Connector. The outputs are 10 LEDs, and the JTAG UART Debug Console. The system above can be created in Qsys using a standard library of re-useable IP blocks. The System Interconnect Fabric is automatically generated by Qsys and binds the blocks together. The system interconnect manages dynamic bus-width matching, interrupt priorities, arbitration and address mapping. This system is a full-featured processor system capable of running operating systems such as uC-OSII or Linux.

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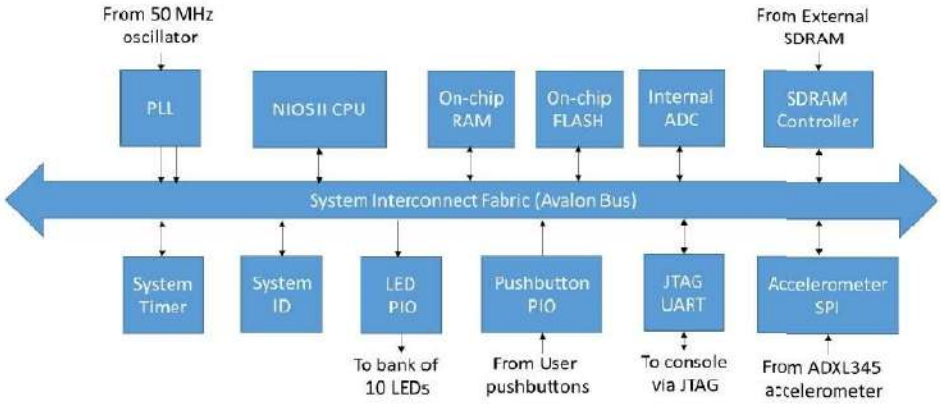

Fig. 1. System Block Diagram

III. COMPONENTS

A. DE10-Lite

The DE10-Lite presents a robust hardware design platform built around the Altera MAX 10 FPGA. The MAX 10 FPGA is well equipped to provide cost effective, single-chip solutions in control plane or data path applications and industry-leading programmable logic for ultimate design flexibility. With MAX 10 FPGA, you can get lower power consumption / cost and higher performance. When you need high-volume applications, including protocol bridging, motor control drive, analog to digital conversion, image processing, and handheld devices, the MAX 10 Lite FPGA is the best choice. Th DE10-Lite is a FPGA evaluation kit that is designed to get you started with using an FPGA. The DE10-Lite adopts Altera's non-volatile MAX® 10 FPGA built on 55-nm flash process. MAX 10 FPGAs enhance non-volatile integration by delivering advanced processing capabilities in a low-cost, instant-on, small form factor programmable logic device. The devices also include full-featured FPGA capabilities such as digital signal processing, analog functionality, Nios II embedded processor support, and memory controllers.

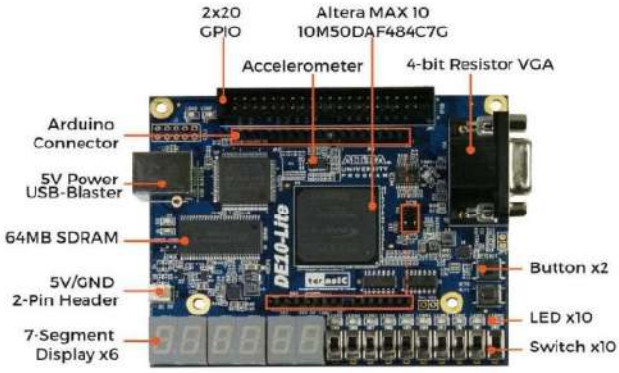

Fig. 2. DE-10 Lite Board

The DE10-Lite includes a variety of peripherals connected to the FPGA device, such a 8MB SDRAM, accelerometer, digital-to-analog converter (DAC), temperature sensor, thermal resistor, photo resistor, LEDs, pushbuttons and several different options for expansion of connectivity through GPIO

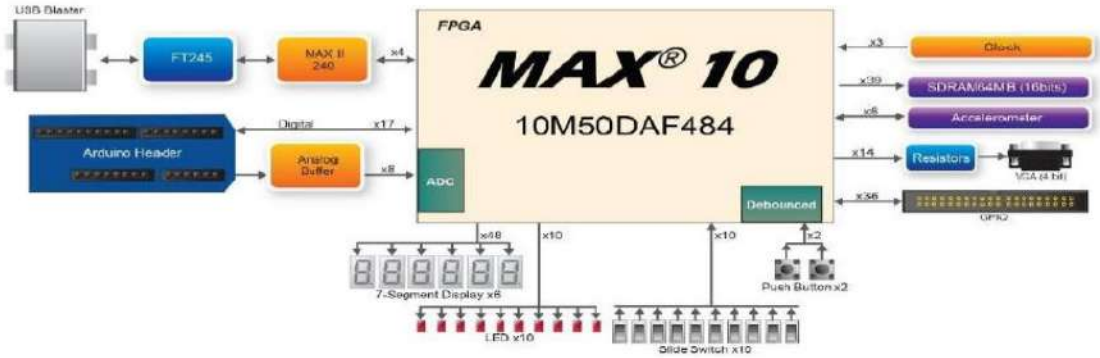

Fig. 3. Board Block Diagram

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IV. GENERAL DESIGN FLOW

The DE10-Lite System Builder will generate two major files, a top-level design file (.v) and a Quartus II setting file (.qsf) after users launch the DE10-Lite System Builder and create a new project according to their design requirements. The top-level design file contains a top-level Verilog HDL wrapper for users to add their own design/logic. The Quartus II setting file contains information such as FPGA device type, top-level pin assignment, and the I/O standard for each user-defined I/O pin. Finally, the Quartus II programmer is used to download .sof file to the development board via JTAG interface

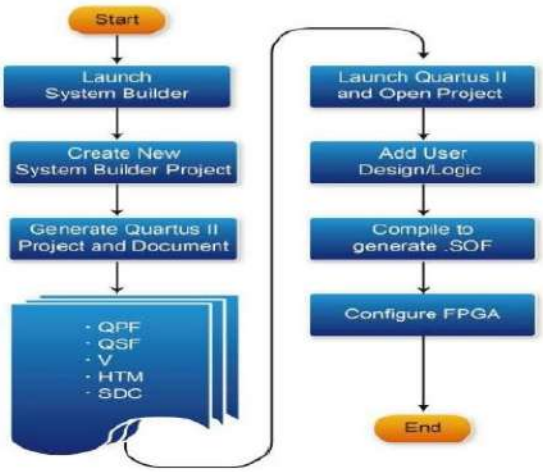

Fig. 4 . Design flow of building a project from the beginning to the end

V. HARDWARE / SOFTWARE REQUIREMENTS

Hardware Requirements of the Project

- ☐ Intel Altera MAX10 DE-10 Lite FPGA Board

Software Requirements of the Project

- ☐ Altera Quartus Prime Ver ion 16.1 FPGA Development Software Tool
- ☐ Altera System Design Tool Qsys (Platform Builder)
- ☐ Altera NIOS II SBT for Eclipse

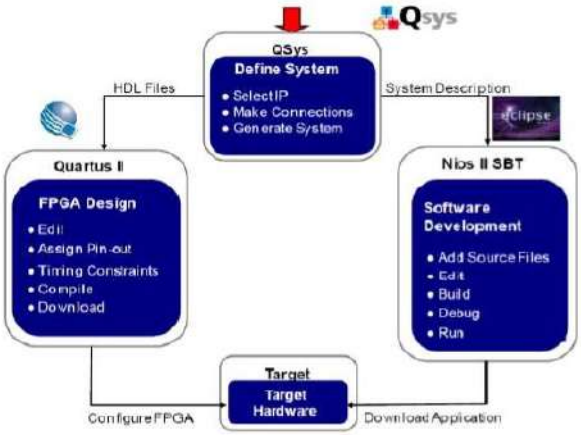

Fig. 4 . System tool flow

VI. SYSTEM DESIGN PROCESS

All the IP blocks given in the Fig.1 are added to the Qsys (The System Builder Software) and are asiigned with their respective clocks and resets.

Component	Input Clock Frequency	Source	Designation
1. SDRAM PLL	50 MHz	Oscillator on DE10-Lite	MAX10_CLK1_50
2. Nios II processor and peripherals	80 MHz	Output 'c0' of PLL	sdram_pll_c0
3. SDRAM phase shifted clock	80 MHz (-90° phase)	Output 'c1' of PLL	sdram_pll_c1
4. Slow Peripherals	40 MHz	Output 'c2' of PLL	pll_c2
5. ADC PLL	10 MHz	Oscillator on DE10-Lite	ADC_CLK_10
6. internal ADC	10 MHz	Output 'c0' of ADC PLL	adc_pll_c0

Fig. 5. Clocking Scheme

After all the connections were made and system configurations such as Clocks,IRQ's,Resets,BaseAdresses are given the final Qsys will like this.

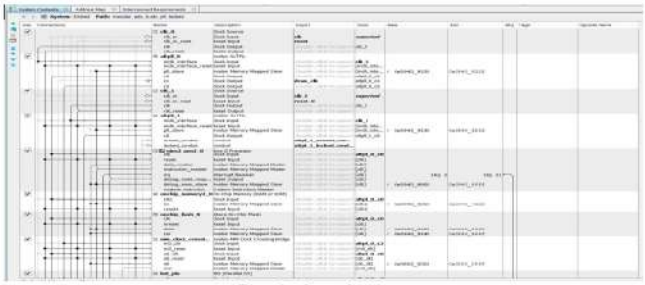

Fig. 6. Qsys System

VII. COMPILATION AND SYNTHESIS

HDL files related to the System are generated and then the project is compiled and after successful compilation look at the Flow Messages. Note that there are tabs at the top of the messages window that allow you to filter by message type. Look at the TimeQuest Timing Analyzer, Slow 1200mV 85C Model, Fmax Summary to determine the Fmax. Look at the Flow summary to determine the total registers (Flip-Flops) and % utilization of logic elements

Slow 1200mV 85C Model Fmax Summary

<<Filter>>

	Fmax	Restricted Fmax	Clock Name
1	50.38 MHz	50.38 MHz	ADC_CLK_10
2	62.15 MHz	62.15 MHz	altera_reserved_tck
3	86.0 MHz	86.0 MHz	p1|altpll_component|auto_generated|pll1|clk[0]
4	100.81 MHz	100.81 MHz	u3|altpll_0|sd1|pll7|clk[2]
5	103.72 MHz	103.72 MHz	u3|altpll_0|sd1|pll7|clk[0]
6	228.26 MHz	228.26 MHz	MAX10_CLK1_50
7	272.03 MHz	272.03 MHz	p1|altpll_component|auto_generated|pll1|clk[1]
8	364.17 MHz	250.0 MHz	MAX10_CLK2_50

Fig. 7 . Fmax Summary

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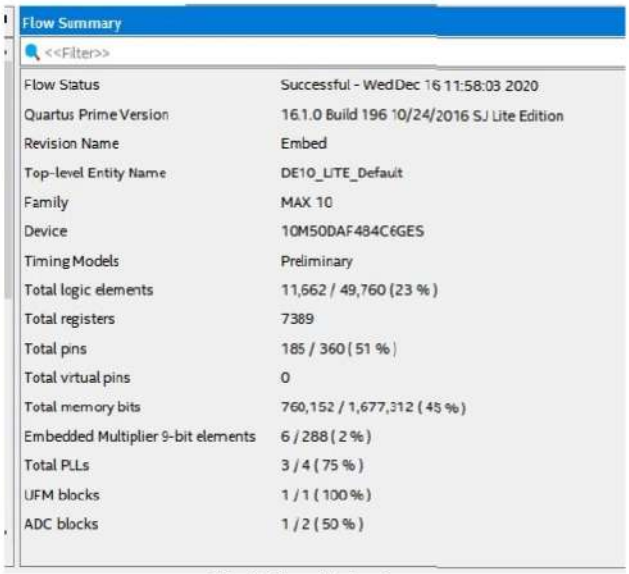

Flow Summary	
<<Filter>>	
Flow Status	Successful - Wed Dec 16 11:58:03 2020
Quartus Prime Version	16.1.0 Build 196 10/24/2016 SJ Lite Edition
Revision Name	Embed
Top-level Entity Name	DE10_LITE_Default
Family	MAX 10
Device	10M50DAF484C6GES
Timing Models	Preliminary
Total logic elements	11,662 / 49,760 (23 %)
Total registers	7389
Total pins	185 / 360 (51 %)
Total virtual pins	0
Total memory bits	760,152 / 1,677,312 (45 %)
Embedded Multiplier 9-bit elements	6 / 288 (2 %)
Total PLLs	3 / 4 (75 %)
UFM blocks	1 / 1 (100 %)
ADC blocks	1 / 2 (50 %)

Fig. 8. Compilation Report

Fig. 9. Software Console Report

VIII. CONCLUSION

We have designed a system with high performance NIOS-2 processor successfully which is implemented on FPGA development kit.We know that performance of any system can be known by the number of operations it is performing per second that is nothing but the Frequency (Fmax).

So the performance boost can be clearly observed from the compilation reports. Hence this kind of implementation can further be used for various emerging applications like 5G, Edge computing, Cyber Security etc.The number of soft core processors and hardware development platforms are available in the market. The outcome of the present research work related to significant improvement in performance measure and the choice of wide variety of available resources in the design of development environment encourages one to extend the suggested methodology to any general application.

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