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Parasitic Aware Automatic CMOS Analog Circuit Design using Evolutionary Algorithm

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Title

Parasitic Aware Automatic CMOS Circuit using Evolutionary Algorithms.

1 Abstract

In this work, we propose a novel concept of the parasitic-aware automatic CMOS circuit design. Further, two efficient evolutionary algorithms namely; EABC (Efficient Artificial Bee Colony) algorithm and MPSO (Modified Particle Swarm Optimization) algorithm are proposed. In order to overcome the problem of loss of diversity in PSO (Particle Swarm Optimization) algorithm, MPSO algorithm uses a partial re-initialization technique. In the EABC algorithm, the issue of the poor exploitation of ABC (Artificial Bee Colony) algorithm is addressed. The MPSO, PSO, ABC and EABC algorithms are used to carry out the schematic-level design of the:(1) Two-stage operational amplifier, (2) high-gain low voltage bulk-driven OTA, and (3) second generation current conveyor. The design is carried out in the $0.13\mu m$ and $0.09\mu m$ CMOS technologies. The obtained results reveal the effectiveness of the proposed algorithms to design analog CMOS circuits. The ABC algorithms designed two-stage op-amp in $0.13\mu m$ CMOS technology with an error of 1.01% while the EABC algorithm designed opamp with an error of only 0.39%. The ABC algorithm designed high gain OTA with 0.69% error, while MPSO algorithm designed the same circuit with 0% error. In order to investigate the effect of the layout parasitic on the performance on the circuit, the layout of opamp was prepared based on schematic level optimization. The post-layout simulation indicated that, The performance of circuit at layout-level was degraded by 6% due to the layout parasitic. In order to overcome this problem and to achieve parasitic-aware automatic circuit design, the concept of the schematic-level automatic circuit design is extended to the layout-level by utilizing layout in the design process. To achieve this, use of the configurable layouts is proposed instead of the conventional handcrafted layouts. Unlike conventional handcrafted layouts, the configurable layouts allow the user to change the size of various components of layout and the distances between them automatically by changing the parameters of the layout. This feature of the configurable layout makes them flexible and suitable for use in automatic circuit design framework. The configurable layouts are developed using MAGIC VLSI Tool. The automatic parasitic-aware design of the: (1) Two stage operational amplifier, (2) Bulk-driven OTA, (3) Ring oscillator, (4) Voltage controlled oscillator and (5) Inverter buffer are carried in this work. The proposed concept does not require any human intervention and provides a layout of designed circuit. Further, it has also been demonstrated that process variations can also be considered in the design cycle. The design of two-stage op-amp and OTA is carried out taking into account process variations.

2 Introduction

In recent years, with the increase of complexity, the design of the analog and mixed signal CMOS integrated circuits in an efficient manner is a critical task. In order to handle the complexity of integrated circuits, hierarchical blocks oriented design approach is used widely. For the analog CMOS circuits, such hierarchical blocks are generally amplifiers, filters, references, mixers, and oscillators. The design of these building blocks includes sizing of various MOSFETs to achieve target design specifications such as power consumption, gain, bandwidth, slew rate. Since the performance of such analog circuits is very sensitive to design parameters, their design requires lots of expertise. The analog circuit design process is a knowledge intensive trade-off approach [1].

The traditional analog circuit design is carried out in three steps: (1) Topology selection, (2) Component sizing i.e. schematic-level design, and (3) Layout extraction i.e. layout-level design [2]. During the schematic-level design, generally, analytical calculations are followed by the circuit simulations. The BSIM models are used widely in simulation to describe the behavior of MOSFET. There are more than 150 parameters in level 54 BSIM model for the consideration of various short-channel effects of the MOSFET. It is very difficult to consider all these parameters in analytical calculations. Thus, the schematic-level design largely depends upon simulations. In order to overcome these difficulties and to achieve time-efficient design, many researchers have successfully applied heuristic and classical optimization techniques in schematic-level circuit design [3–12].

In the layout-level design phase, based on the schematic-level design, layouts are prepared. Due to the immense complexity, the analog circuit has not been automated like the digital design [13]. Since the layout adds parasitic components to the circuit, there is a difference in the simulation of schematic-level design and layout-level design, especially, in frequency sensitive specifications such as bandwidth and slew rate. The unacceptable difference in simulation results leads redesigning of the circuit. The efficient approach for the designing analog CMOS circuit is required to overcome these difficulties. Further, the concept of the automatic CMOS analog design is only limited to schematic-level and not yet applied to layout-level to handle layout-parasitics in the design process.

3 Problem definition

The aim of this research work is to develop a time-efficient method for the design of the high-performance analog CMOS circuits at layout-level. Many researchers have successfully applied optimization algorithms to efficiently design CMOS analog circuits such as comparator, operational amplifier, differential amplifier, inverter, low noise amplifier, current conveyor, and OTA. However, their design is limited to schematic-level. The schematic-level design cannot consider the final design because in this design process,

layout parasitics are not considered and the exact value of the layout parasitics cannot be estimated. The irregularities in the device dimensions prevent the use of the automatic placement and routing tools for preparing the layouts of analog circuits, and hence, the layouts for analog circuits are prepared manually. Sometimes, the small change in such layouts may require large efforts. Due to such limitations, the traditional design approach fails to provide a time-efficient design for the analog circuits.

To overcome this problem, the concept of the configurable layouts is proposed. The configurable layouts allow the user to change various parameters of the layout. This flexibility of the configurable layout allows the use of the optimization algorithms to carry out layout-level design where the exact consideration of parasitic is possible. Thus, the use of the configurable layouts enables the consideration of all kinds of parasitics from the beginning of the circuit design process and allows parasitic-aware design automation for the analog CMOS circuits. Further, this work also proposes improved evolutionary algorithms for the analog CMOS circuit design problem.

4 Objective and scope of work

Objective

- To propose an approach for the time-efficient parasitic-aware layout-level design automation of the analog CMOS circuits.
- To propose efficient evolutionary optimization algorithms for the analog circuit design.

Scope of work

- To develop efficient evolutionary optimization techniques.
- To design standard analog CMOS circuit at schematic-level amplifier against various design specifications using proposed evolutionary algorithms.
- To compare performance of proposed evolutionary techniques with the existing standard evolutionary algorithms for the analog CMOS circuit deign problem.
- To develop a framework for the parasitic-aware analog CMOS circuit design.
- To demonstrate parasitic-aware design using proposed approach by designing analog CMOS circuits.

5 Contribution

The automatic design of the analog CMOS circuits is carried out using classical optimization algorithms, geometric programming technique, and evolutionary algorithms. However, the circuit design is confined to the schematic level only and parasitic effects are not considered. Further, it is not possible to estimate exact value of the parasitic. The following is the contribution from this work.

- Two efficient evolutionary algorithms: (1) EABC (Enhanced Artificial Bee Colony) algorithm, and (2) MPSO (Modified particle swarm optimization) are proposed for the CMOS circuit design and optimization.
- Three circuits namely: (1) Two-stage operational amplifier, (2) High gain bulk-driven OTA, and (3) Second generation current conveyor are designed at schematic level using MPSO, PSO, ABC, and EABC algorithms in $0.13\mu m$ and $0.09\mu m$ CMOS technologies.
- The concept of the automatic circuit design is extended from schematic-level to layout-level by proposing configurable layouts.
- The framework for the configurable layout is developed using MAGIC VLSI Tool
- The automatic parasitic-aware designs of: (1) Two-stage operational amplifier, (2) Bulk-driven OTA, (3) Ring oscillator, (4) Inverter buffer, and (5) VCO are carried out using proposed concept
- The process and temperature variations are also considered in the automatic design of the two-stage operational amplifier.

6 Automatic analog circuit design

The integrated circuit design process flow is shown in Fig. 1. The design process can be divided into the following three steps: (1) Topology selection, (2) Schematic-level design, and (3) Layout-level design. Due to the short-channel effects and the non-linearities of the device, traditional design process fails to provide a solution efficiently. In order to design high-performance analog circuits time efficiently, researchers have applied classical and evolutionary algorithms based optimization techniques at schematic-level. The examples of classical optimization techniques used for the circuit design are linear programming [3], dynamic programming [4], sequential programming [5], steepest descent method. However, such classical optimization algorithms suffer from following problems. The quality of the solution depends on the starting point and in the absence of good starting-point,

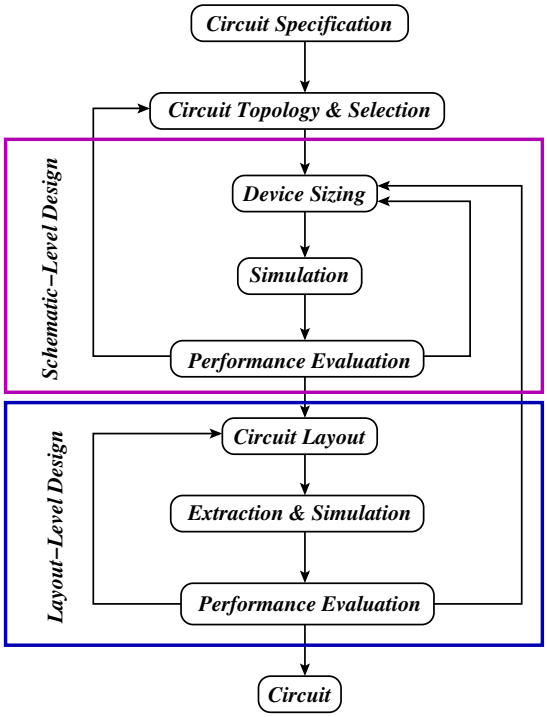


Figure 1: Analog integrated circuit design process flow

the algorithms may provide a locally optimized solution. Further, such algorithms require accurate objective function [11]. The formulation of the accurate objective function for the analog circuit design is very difficult. The complexity of the optimization technique based on the dynamic programming increases exponentially with the size of the problem [14]. Many researchers have used Geometric programming technique to design operational amplifier and comparator. The geometric programming requires models to prepare constrains. When the short-channel effects are not negligible, it is very difficult to develop such models [11]. The Genetic algorithm (GA), particle swarm optimization (PSO), artificial bee colony (ABC) algorithm, differential evolution (DE) are some of the widely used evolutionary algorithms. These algorithms are easy to implement using programming techniques. The output of the simulator can be utilized in the optimization process eliminating the need for circuit-specific cost function. These advantages of the evolutionary algorithms make them popular for the design of the analog CMOS circuits.

6.1 Automatic analog circuit design at Schematic-level

The design parameters for the analog CMOS circuits are generally width and length of various MOSFETs. The optimization algorithm determines the values of these parameters so that desired specifications can be achieved. The conceptual block diagram for the schematic-level circuit optimizer using ABC algorithm is given in Fig. 2. The search space generally represents upper and lower bounds for the design parameters. The proper

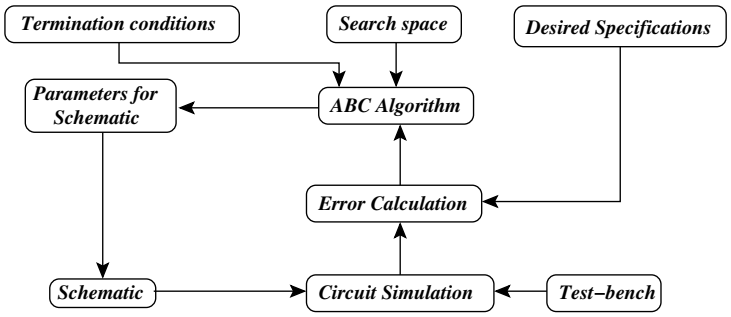


Figure 2: Conceptual block diagram for automatic analog circuit design at schematic-level

search-space avoids generation of non-practical solutions. The optimization algorithm generates a solution from the search space. Based on this solution, the circuit is simulated against pre-determined test-bench, and simulation results are analyzed to calculate the error. This error is utilized by the algorithm to generate new solutions. The aim of the algorithm is to minimize error. This is an iterative process and continue till all specifications are not satisfied or termination criteria are not met.

To calculate error, we use Root-Mean-Square (RMS) error formula as suggested in [11].

$$RMS\ error,\ f_e(\%) = \sqrt{\frac{1}{N}\sum_{i=1}^{N} E_i} \times 100 \tag{1}$$

$$E_i = \begin{cases} 0 & \text{if } i^{th} \text{ specification is satisfied} \\ \left(\frac{OS_i - DS_i}{DS_i}\right)^2 & \text{Otherwise} \end{cases}$$

where, N is total number of specifications, DS_i is i^{th} desired specification and OS_i is i^{th} obtained specification from simulation. If, the solution candidate generates layout with DRC error, the solution is discarded and large error is passed to the algorithm for the concerned solution candidate.

For the circuit design and optimization, we utilized PSO and ABC algorithms and proposed MPSO (Modified Particle swarm optimization) algorithm and EABC (Enhanced artificial bee colony) algorithm.

The PSO algorithm is very popular for solving the engineering problems. It simulates the behavior of birds flocks searching for food [15]. In this algorithm, each particle represents a solution candidate. Each particle is assumed to move in search space with the certain velocity. The new velocity of the particle is calculated based on best position ever visited by the particle and overall best solution found during the journey of the particle up to the present time. The convergence speed of PSO algorithm is fast, however, it suffers from saturation problem due to loss of swarm diversity and likely to trap in locally optimized solution [16]. The MPSO algorithm addresses this problem of the PSO algorithm. In MPSO algorithm, the novel re-initialization scheme is used to avoid saturation

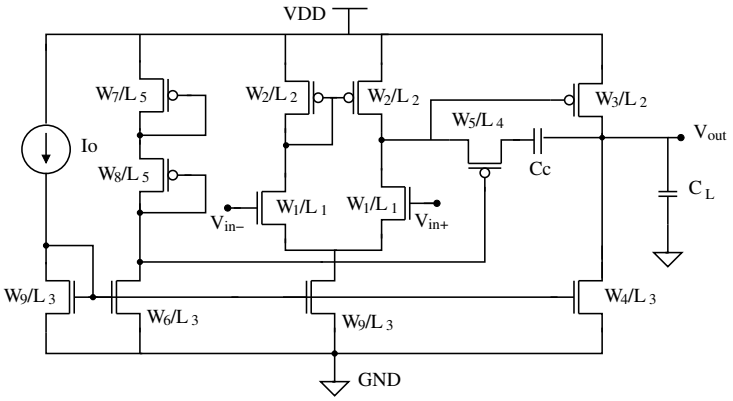


Figure 3: Circuit of Two-stage Op-amp

of algorithm. This avoids trapping of the algorithm in locally optimized solution.

The performance comparison of ABC, PSO, DE and swarm-inspired evolution algorithm (PS-EA) algorithms based on their ability to solve benchmark functions reveals that the performance of the ABC algorithm is superior, and it also requires the fewer number of control parameters [17] [18]. However, due to poor exploitation ability, ABC algorithm suffers from the slower convergence speed. The EABC algorithm is based on the ABC algorithm. The new search strategy used in EABC algorithm improves exploitation ability of algorithm and improves its convergence speed.

In order to evaluate the performances of the EABC and MPSO algorithms, we designed following circuits in $0.13\mu m$ and $0.09\mu m$ CMOS technologies using these algorithms.

- Two stage CMOS Operational-amplifier
- High gain bulk driven OTA
- Second generation current conveyor (CCII)

Further, these circuits are also designed using ABC, PSO, GABC [19] and MABC [20] algorithms and obtained results are compared. Each circuit is designed 10 times independently and average results are considered for comparison. The maximum circuit evaluations during the design process are set to 5000. We use NG-SPICE [21] as circuit simulator and utilize PTM device models [22]. The experiment is conducted on computer having following major specifications: Processor - AMD FX-8350; Clock - 4GHz, RAM - 4GB, OS - Ubuntu 12.04-64 bits, Kernal - 3.13.0-95-generic.

6.1.1 Two Stage Operational Amplifier

The two-stage amplifier is widely used in the analog integrated circuits. It is a building block of many other circuits such as amplifiers, mixer, filter, ADC, and DAC. The circuit of the two-stage op-amp is shown in Fig. 3 [23]. The design parameters are width and length of the various transistors, the value of the bias current and value of Miller

Table 1: Two-stage op-amp: Search space for the design parameters

Parameter	Search space ($0.13\mu m$)	Search space ($0.09\mu m$)
W_1 to W_9	0.5 μm to 10 μm	0.5 μm to 10 μm
L_1 to L_5	0.2 μm to 1 μm	0.1 μm to 1 μm
I_0	1 μA to 10 μA	1 μA to 10 μA
C_C	0.001pF to 1pF	0.001pF to 1pF
VDD (Fixed)	1.2V	1.0V

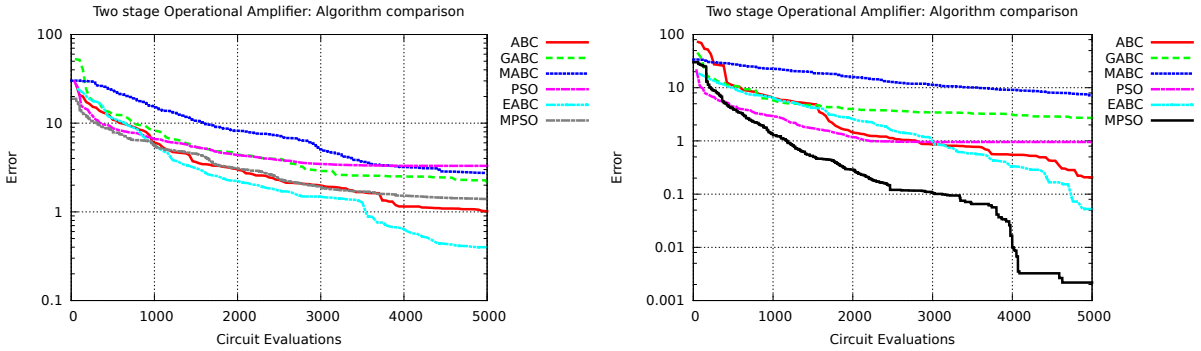
Table 2: Two stage operational amplifier (Schematic-level): Performance comparison of algorithms based on 10 independent design runs.

	Technology	ABC	GABC	MABC	PSO	EABC	MPSO
Average RMS error(%)	$0.13\mu m$	1.01	2.02	2.71	3.30	**0.39**	1.39
	$0.09\mu m$	0.20	2.71	7.18	0.95	0.05	**0.002**
Worst RMS error(%)	$0.13\mu m$	5.77	6.74	8.84	6.80	**1.97**	2.11
	$0.09\mu m$	0.58	5.62	21.2	4.68	0.52	**0.02**
Average circuit evaluations	$0.13\mu m$	4482	**3604**	5000	5000	3608	4680
	$0.09\mu m$	4720	5000	5000	4406	3500	**2946**
Average design time (Minutes)	$0.13\mu m$	39.6	**31.2**	40.7	43.2	36.2	41.1
	$0.09\mu m$	16.41	17.3	15.9	15.8	12.2	**10.8**
Number of times zero RMS error is obtained	$0.13\mu m$	3	**5**	0	0	**5**	1
	$0.09\mu m$	3	0	0	2	**9**	**9**

capacitor. There are 16 design parameters. The search-space for the design parameters are described in Table 1. The desired specifications are as follows; Gain $\geq 80dB$, Unity gain bandwidth (UGB) $\geq 100MHz$, Phase margin (PM) $\geq 60°$, Power consumption (PC) $\leq 20\mu W$, Rise and fall slew rate (RSR) $\geq 40V/\mu S$, Power supply rejection ratio (PSRR) $\geq 75dB$, Common-mode rejection ratio (CMRR) $\geq 80dB$. The average of obtained results over 10 independent runs are shown in Table 2. The obtained results reveal that the both proposed algorithms EABC and MPSO algorithms perform efficiently than other considered algorithms. In Fig. 4, the variations in the RMS error with the circuit evaluations are shown. This helps to compare convergence speed of the considered algorithms. The EABC algorithm design op-amp in $0.13\mu m$ technology most efficiently, however, the MPSO algorithm is performing better for design in $0.09\mu m$ technology. In Table 3, simulation of best designs obtained during 10 independent run in $0.13\mu m$ CMOS technology using EABC algorithm and MPSO algorithm are shown.

6.1.2 High gain bulk driven OTA

The operational transconductance amplifier (OTA) is widely used in analog circuits. It is a building block of the gm-C filter, data converters, active inductor, and resistors. In this work, high-gain bulk-driven OTA is designed. In the bulk-driven technique, the input signal is applied to the bulk terminal of the MOSFET. This helps to overcome limitation



(a) 0.13μm CMOS technology (b) 0.09μm CMOS technology

Figure 4: Two stage op-amp: Variation in RMS error with circuit evaluations

Table 3: Two-stage op-amp (0.13μm CMOS technology): Simulation result of best design obtained by EABC algorithm and MPSO algorithm

	Specifications	EABC	MPSO
Gain (dB)	≥ 80	80.0	85.7
PM (°)	≥ 60	72.1	60.8
UGB (MHz)	≥ 100	107.5	143.3
PSRR (dB)	≥ 75	84.1	79.2
CMRR (dB)	≥ 80	82.8	110.0
PC (μW)	≤ 20	19.6	19.4
RSR ($V/\mu S$)	≥ 40	47.2	83.0
FSR ($V/\mu S$)	≥ 40	40.1	40.3
Error (%)	$= 0$	0.0	0.0

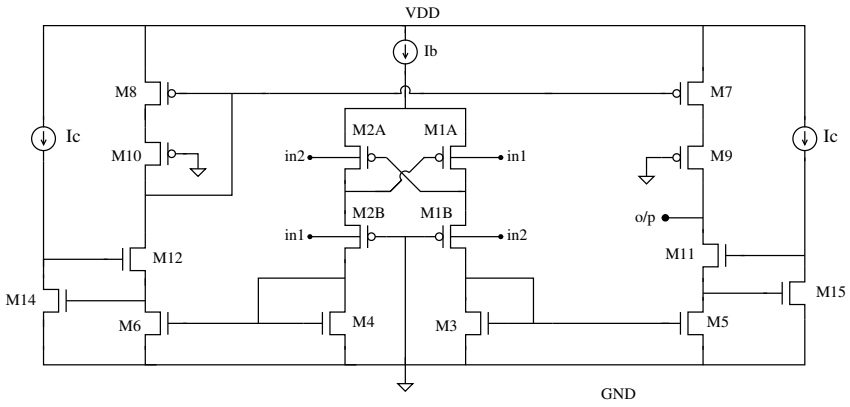


Figure 5: Circuit of High-gain bulk-driven OTA

Table 4: High-gain bulk-driven OTA: Search space for the design parameters

Parameter	Search space (0.13μm)	Search space (0.09μm)
Width(W) of each transistor	1 μm to 100 μm	1 μm to 100 μm
Length(L) of each transistor	0.2 μm to 2 μm	0.1 μm to 2 μm
I_b	0.1 μA to 2 μA	0.1 μA to 2 μA
I_c	0.1 μA to 1 μA	0.1 μA to 1 μA
VDD	0.5V	0.5V

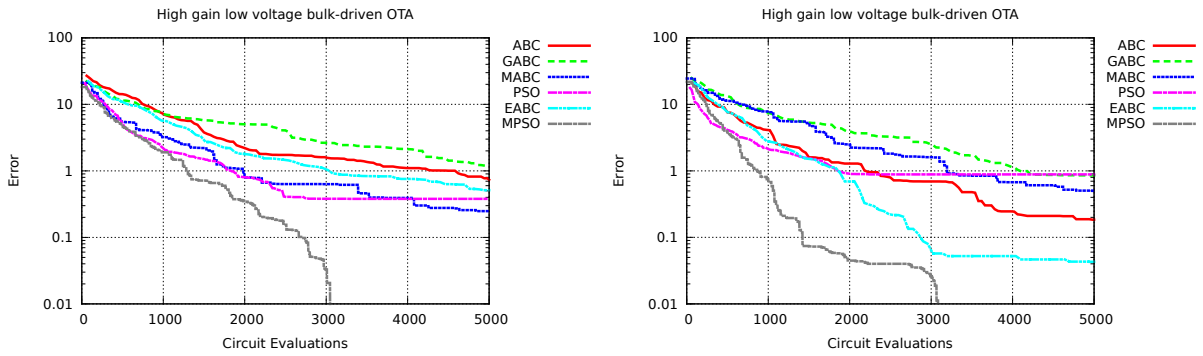
Table 5: High gain low voltage bulk-driven OTA: Performance comparison of algorithms based on 10 independent design runs.

	Technology	ABC	GABC	MABC	PSO	EABC	MPSO
Average RMS error(%)	$0.13\mu m$	0.69	1.18	0.16	0.37	0.51	**0.0**
	$0.09\mu m$	0.18	0.85	0.48	0.88	0.04	**0.0**
Worst RMS error(%)	$0.13\mu m$	1.64	3.98	1.42	3.74	1.88	**0.0**
	$0.09\mu m$	0.96	4.16	2.46	5.51	0.42	**0.0**
Average circuit evaluations	$0.13\mu m$	4148	4096	1991	2012	3950	**1572**
	$0.09\mu m$	3212	4700	3097	2002	2396	**932**
Average design time (Minutes)	$0.13\mu m$	55.8	53.5	28.4	32.8	53.6	**27.3**
	$0.09\mu m$	44.5	59.9	38.0	28.8	32.7	**13.9**
Number of times zero RMS error is obtained	$0.13\mu m$	3	4	8	8	6	**10**
	$0.09\mu m$	7	3	6	8	9	**10**

Table 6: High-gain bulk-driven OTA ($0.13\mu m$ CMOS technology): Simulation result of best design obtained by EABC algorithm and MPSO algorithm

	Specifications	EABC	MPSO
Gain (dB)	≥ 80	81.5	81.2
PM (°)	$\geq$ 60	61.3	64.0
UGB (MHz)	≥ 1.5	2.1	2.0
PC (μW)	≤ 5	4.2	3.7
RSR (V/mS)	≥ 0.1	0.28	0.18
FSR (V/mSS)	≥ 0.1	0.29	0.18
Error (%)	$= 0$	0.0	0.0

imposed by the threshold voltage. The bulk-driven technique is quite useful for building low voltage bio-medical circuits. However, transconductance offered by the bulk-driven technique is significantly less than the gate-driven technique. This results in the low gain. The circuit of designed bulk-driven OTA is shown in Fig.5. The cross-coupled pair used imparts negative impedance for degeneration. This results in enhancement of overall transconductance of the differential pair [24]. The circuit is designed in both $0.13\mu m$ and $0.09\mu m$ CMOS technologies using ABC, GABC, MABC, PSO and MPSO algorithms with following specifications; Gain $\geq 80(dB)$, Unity gain bandwidth (UGB) $\geq 1.5MHz$, Phase margin (PM) $\geq 60°$, Power consumption (PC) $\leq 5\mu W$, Rise and fall slew rate (RSR) $\geq 0.1V/\mu S$. The average of the obtained results over 10 independent runs are shown in Table 5. In Fig. 6 , the variation in the RMS error with the circuit evaluations is shown. The obtained results reveals that the MPSO algorithm is able to design OTA most efficiently. In Table 6, simulation of best designs obtained during 10 independent run in $0.13\mu m$ CMOS technology using EABC algorithm and MPSO algorithm are shown.



(a) 0.13μm CMOS technology (b) 0.09μm CMOS technology

Figure 6: High-gain bulk-driven OTA: Variation in RMS error with circuit evaluations

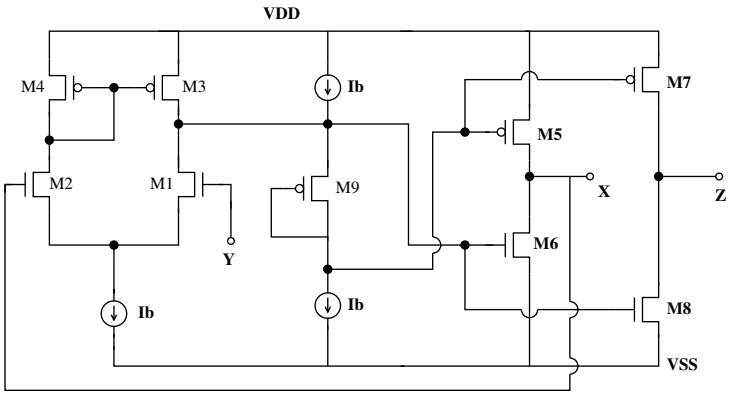


Figure 7: Circuit of low-voltage CCII

6.1.3 Low voltage second generation current conveyor (CCII)

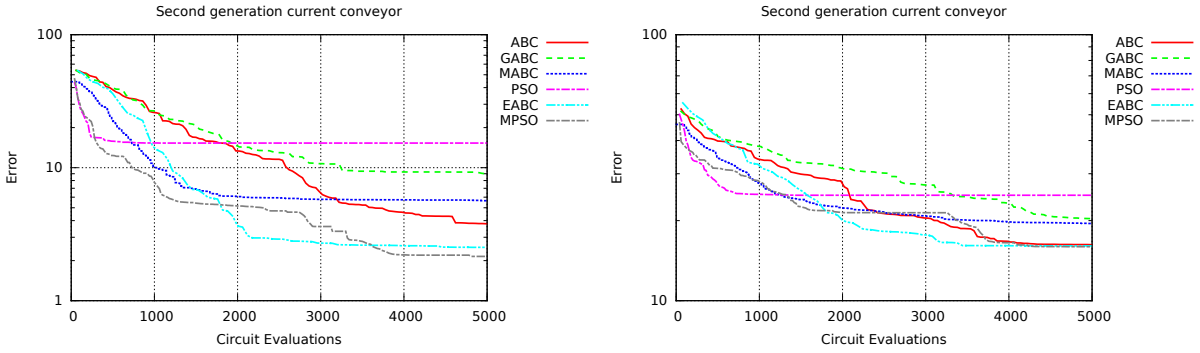
The current conveyor circuit was proposed by Sendra [25] and it is a building block of many current mode signal processing circuits. The current conveyor can be utilized for voltage to current converter, current to voltage converter, voltage controlled voltage amplifier, voltage controlled current source, current amplifier, current differentiator and current integrator. Further, it is a building block of current feedback operational amplifier and active filters [26]. We designed low voltage positive second generation current conveyor(CCII+) as shown in Fig. 7 [27]. The search-space for the design parameters are shown in Table 7. The design specifications are as follows; Voltage gain = 1, Current gain = 1, Voltage bandwidth $\geq 500MHz$, Current bandwidth $\geq 500MHz$, Impedance of X terminal, $Z_x \leq 50\Omega$, Impedance of Z terminal, $Z_z \geq 100K\Omega$, Power consumption (PC) $\leq$

Table 7: Low voltage CCII: Search space for design variables.

Parameter	Search space (0.13μm)	Search space (0.09μm)
Width(W) of all transistors	1 μm to 100 μm	1 μm to 100 μm
Length(L) of all transistors	0.2 μm to 2 μm	0.1 μm to 2 μm
I_b	1 μA to 50 μA	1 μA to 50 μA
VDD	0.8V	0.6V

Table 8: Low voltage CCII: Performance comparison of algorithms based on 10 independent design runs.

	Technology	ABC	GABC	MABC	PSO	EABC	MPSO
Average RMS error(%)	$0.13\mu m$	3.78	9.02	5.64	15.32	2.51	**2.15**
	$0.09\mu m$	16.14	20.34	19.51	24.91	16.08	**15.95**
Worst RMS error(%)	$0.13\mu m$	8.86	15.34	6.84	22.46	3.36	**3.02**
	$0.09\mu m$	16.79	36.61	22.63	49.44	16.58	**15.95**
Average circuit evaluations	$0.13\mu m$	5000	5000	5000	5000	5000	5000
	$0.09\mu m$	5000	5000	5000	5000	5000	5000
Average design time (Minutes)	$0.13\mu m$	17.3	17.9	17.3	17.3	**17.0**	17.4
	$0.09\mu m$	17.4	17.8	17.2	17.4	**16.9**	17.6
Number of times zero RMS error is obtained	$0.13\mu m$	0	0	0	0	0	0
	$0.09\mu m$	0	0	0	0	0	0



(a) $0.13\mu m$ CMOS technology (b) $0.09\mu m$ CMOS technology

Figure 8: Low-voltage CCII: Variation in RMS error with circuit evaluations

$200\mu W$. The summary of obtained results over 10 independent runs are shown in Table 8. The variation in the RMS error with the circuit evaluations is shown in Fig. 8. The obtained results shows the effectiveness of EABC and MPSO algorithm.

6.2 Configurable layouts

The handcrafted layouts for the analog circuits are prepared using the graphical interface. Once, the layout is prepared, the distance between various layout components and their size become fixed. Making the change in the prepared layout may require moderate to large efforts. Further, the lifetime of such frozen layout is short as they cannot be ported in other technologies. The configurable layouts on other hand are prepared using the standard macros written in the script file. In the configurable layout, the distances between various layout components, and their dimensions are described using layout parameters or technology dependent variables. This allows making changes in layouts easy. By passing appropriate parameters, new layout can be generated without any human ef-

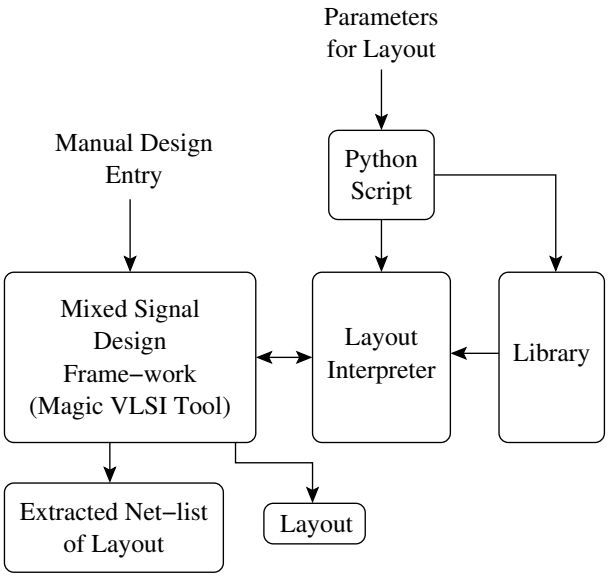


Figure 9: User interface for configurable layout

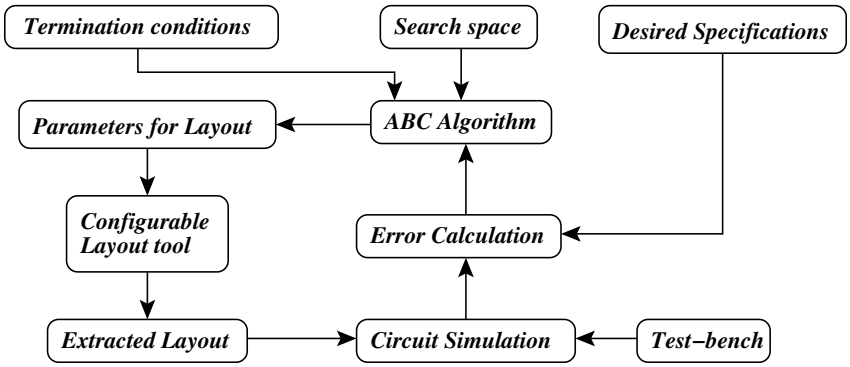
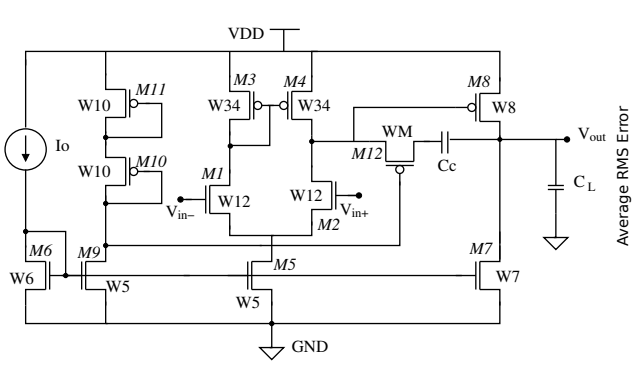


Figure 10: Conceptual block diagram for parasitic aware automatic analog circuit design

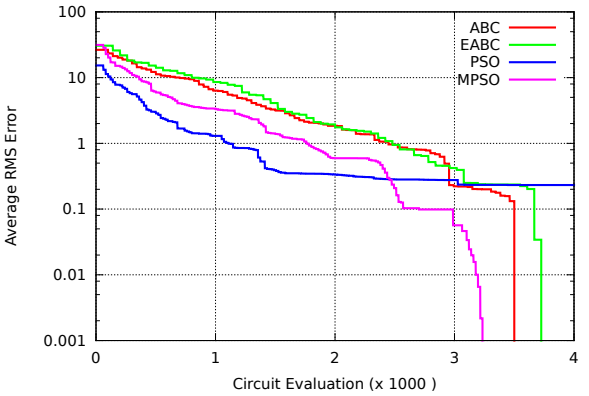
fort. Further, configurable layouts can be easily ported in other technologies very easily. The configurable layouts are prepared for the MAGIC VLSI Tool [28]. The block diagram of design environment for the configurable layout is shown in Fig.9. The script file written in Python programming language [29] is converted into the MAGIC VLSI tool compatible format, and then, the layout tool is triggered to generate layout.

6.3 Parasitic aware automatic circuit design

In order to achieve parasitic-aware automatic circuit design, extracted layout is used instead of the schematic in the optimization process. The configurable layout tool can generate layouts with desired parameters, and generated layout can be extracted into circuit netlist containing all the parasitic components. The conceptual block diagram of the parasitic-aware automatic circuit design is shown in Fig. 10. The algorithm generates parameters for the configurable layout, the configurable layout tool generates the layout and its extracted netlist containing the parasitic component. This extracted lay-



(a) Schematic of two-stage op-amp



(b) Variation in error with layout evaluations

Figure 11: Parasitic-aware design of Two-stage op-amp: (a) Schematic (b) Variation in error with layout evaluations

out is simulated against pre-determined test-bench and error is calculated. Based on this error algorithm generates the new set of parameters. This process continues till termination criteria are not satisfied. This is an automatic process and does not require any intervention.

6.3.1 Parasitic aware design of the two-stage op-amp

The parasitic-aware design of the two-stage op-amp is carried out in the $0.13\mu m$ CMOS technology to drive the load of 0.05pF. The design specifications are as follows: Gain $\geq$ 80 dB; phase margin $\geq 60°$; UGB $\geq$ 100MHz; PSRR $\geq$ 75dB; CMRR $\geq$ 80dB; power consumption $\leq 30\mu W$; Rise and Fall slew rates $\geq 35V/\mu S$. The design parameters are the width of various transistors as shown in the schematic (see Fig. 11a), the length of all transistors and size of the Miller capacitor. To implement capacitor, stacked metal layers are used. The parasitic-aware (layout-level) design of Two-stage op-amp was carried out using ABC, EABC, PSO and MPSO algorithms. The variation in the average RMS error with the circuit evaluations for these algorithms are shown in Fig. 11b. The ABC, EABC, and MPSO algorithms were able to design op-amp all 10 times without any error i.e. all the desired specifications are satisfied. However, the convergence speed of the MPSO algorithm was found faster than other algorithms. In Fig. 12, layout-obtained after the one of the design runs of MPSO algorithm is shown.

Since, there is alway some process variations during the manufacturing process of the integrated circuit, all devices have not exactly the same characteristic. In order to achieve the robust design, it is advisable to consider process variations in the design process. The parasitic-aware automatic design of two-stage op-amp in $0.13\mu m$ technology is also carried out using ABC algorithm considering 10% variation in the process. Further, we also consider the temperature variation between $0°C$ to $70°C$ in the design process. To consider process and temperature variations, five process corners TT, FF, FS, SF, and

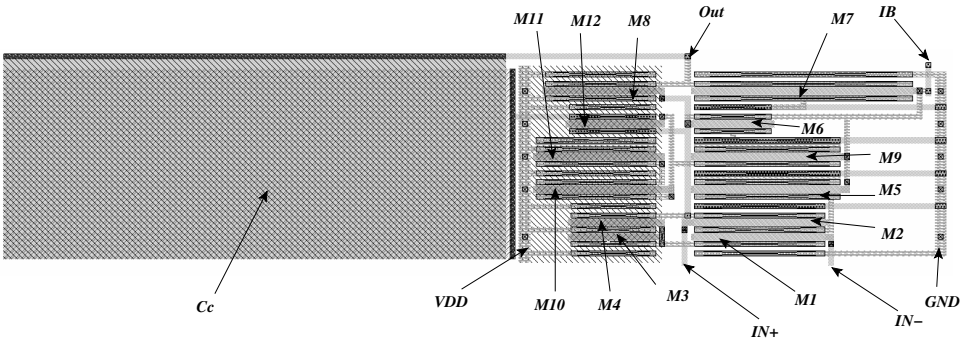


Figure 12: Layout of two-stage op-amp

Table 9: Two stage op-amp ($0.13\mu m$ technology) design using ABC algorithm: Simulation results at different process and temperature corners

Process	Temperature ($^\circ C$)	Gain (dB) ≥ 80	UGB (MHz) ≥ 100	PM ($^\circ$) ≥ 60	PSRR (dB) ≥ 75	CMRR (dB) ≥ 80	PC (μW) ≤ 30	RSR (V/μS) ≥ 35	FSR (V/μS) ≥ 35
TT	0	81.8	137.8	70.3	80.2	82.4	29.6	40.1	36.4
	25	81.2	130.4	67.9	79.2	81.9	29.6	40.1	36.1
	70	80.2	116.8	64.8	77.5	81.2	29.6	40.0	35.8
FF	0	81.6	135.3	72.4	80.5	83.9	29.8	40.4	36.6
	25	81.1	129.2	70.5	79.5	83.6	29.8	40.3	36.4
	70	80.2	117.5	68.0	77.9	83.2	29.8	40.2	36.1
FS	0	81.8	142.6	66.9	78.8	82.1	29.6	40.3	36.6
	25	81.2	132.3	63.9	77.6	81.5	29.6	40.2	36.4
	70	80.2	117.1	60.3	75.5	80.6	29.6	40.1	36.1
SF	0	81.9	128.9	73.4	81.2	83.3	29.5	40.0	35.8
	25	81.3	123.4	71.6	80.3	82.8	29.5	39.9	35.5
	70	80.4	112.6	69.3	78.8	82.3	29.5	39.9	35.3
SS	0	82.1	137.5	68.1	79.9	82.1	29.4	39.9	36.0
	25	81.5	127.7	65.3	78.8	81.5	29.4	39.9	35.8
	70	80.5	113.2	61.9	77.0	80.6	29.4	39.8	35.5

SS are simulated at three temperatures i.e. $0^\circ C$, $25^\circ C$ and $70^\circ C$. The Table 9 illustrates simulation results of designed layout of op-amp using parasitic-aware automatic design approach at the different process and temperature corners. The obtained results clearly indicate effectiveness of the proposed approach of parasitic-aware automatic circuit design.

Other than two-stage op-amp, parasitic-aware designs for the bulk-driven OTA, ring-oscillator, inverter buffer and VCO are carried out in $0.13\mu m$ CMOS technology successfully. In Fig. 13 and Fig. 14 the layouts of bulk-driven OTA and inverter buffer obtained after parasitic-aware design process are shown.

7 Realization of the objectives

- Two efficient algorithms, EABC algorithm and ABC algorithm are proposed. The performances of these algorithms are tested by designing two-stage operational amplifier, high-gain bulk-driven OTA and current conveyor in $0.13\mu m$ and $0.09\mu m$

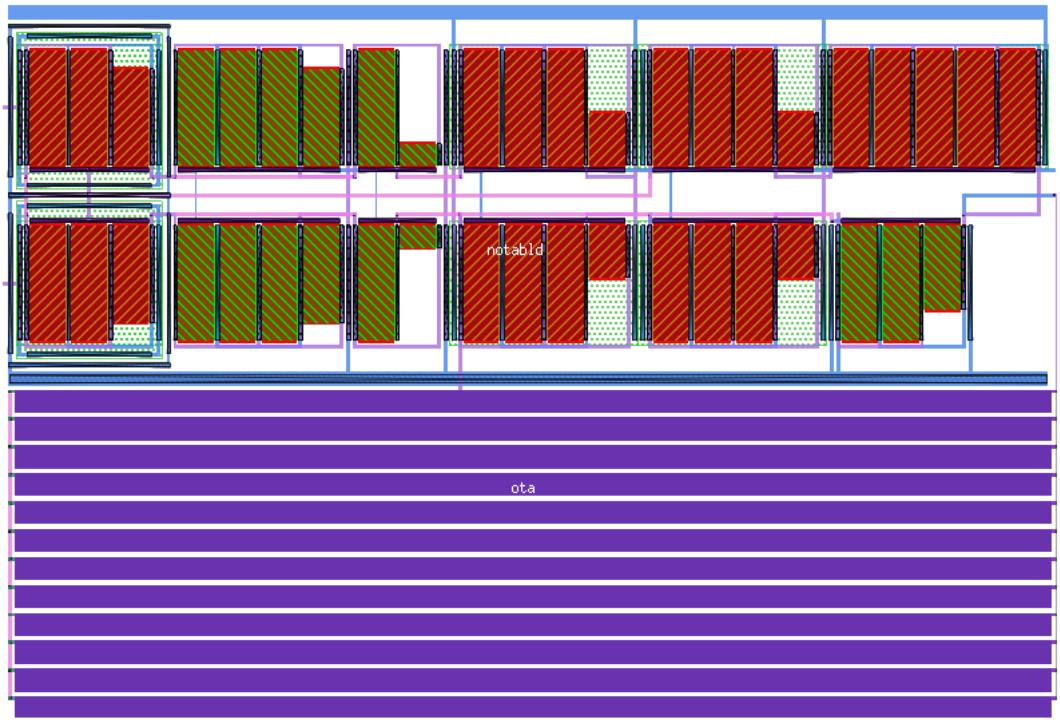


Figure 13: Layout obtained after parasitic-aware design of bulk-driven OTA

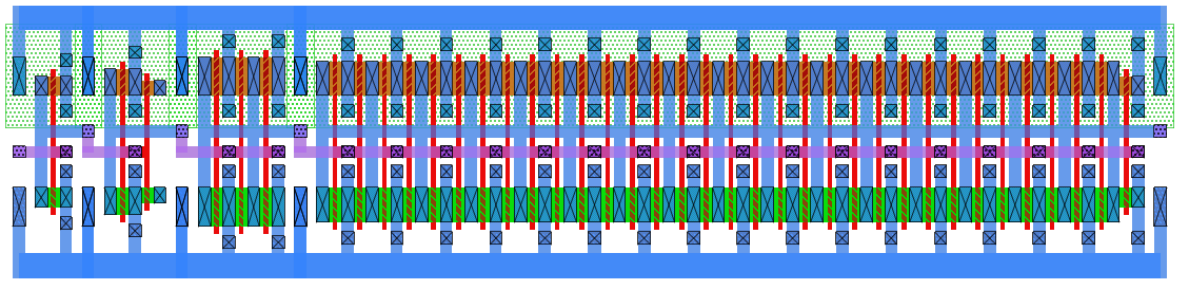


Figure 14: Layout obtained after parasitic-aware design of inverter buffer

CMOS technologies at schematic level.

- The concept of the parasitic-aware automatic circuit design is proposed and verified by designing two-stage operational amplifier, bulk-driven OTA, ring oscillator, inverter buffer and VCO successfully.

8 Conclusion

Two efficient algorithms, EABC and MPSO algorithms are proposed in this work. The performances of these algorithms are compared with ABC, PSO, MABC and GABC algorithms by designing two-stage op-amp, high gain bulk-driven OTA and second generation current conveyor at schematic level in 0.13um, and 0.09um CMOS technology. Both the

proposed algorithms have designed these circuits more efficiently than other considered algorithms. The MPSO algorithm has designed OTA satisfying all the specifications and with zero RMS error. The ABC algorithm has designed OTA with 1.64% error for $0.13\mu m$ technology and 0.96% for the $0.09\mu m$ technology. The PSO algorithm has designed OTA in $0.13\mu m$ technology with 3.74% and 5.51% RMS error.

The concept of an automatic circuit design using evolutionary algorithms is extended to the layout level design by proposing configurable layouts. This enables consideration of all types of parasitics from the beginning of the circuit design. The parasitic-aware automatic circuit design of op-amp in $0.13\mu m$ CMOS technology is demonstrated considering process and temperature variation. The layout of the optimized op-amp is generated successfully without any human intervention. Further, the parasitic-aware design of the bulk-driven OTA, ring oscillator, voltage controlled oscillator and inverter buffer are carried out using the proposed approach. The obtained results reveal the effectiveness of the proposed concept for the layout level design automation.

Publications

1. S. Patel and R. A. Thakker, "Automatic circuit design and optimization using modified pso algorithm," Journal of Engineering Science and Technology Review, vol. 9,no. 1, pp. 89–94, 2016.

Submitted and under review

1. S. Patel and R. A. Thakker, "Parameter Space Exploration for Analog Circuit Design Using Enhanced Bee Colony Algorithm," Journal of Circuits, Systems, and Computers, World Scientific Publishing Company

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