GUJARAT TECHNOLOGICAL UNIVERSITY

Program Name: Master of Engineering
Level: PG
Branch: Electronics And Communication (VLSI Design)
Subject Code: ME02096051
Subject Name: VLSI Test Principles and Architectures

WEF Academic Year	2025-26
Semester	02
Category of the Course	PEC-04

Prerequisite:	Fundamentals of Digital Electronics and CMOS Circuits
Rationale:	It is complex challenges to ensure correct behavior of the whole system-on-chip (SOC) and heterogeneous systems. In this course, the students are able to study basics of fault simulation, ATPG, combinational and sequential circuits, design for testability (DFT) and built-in self-test (BIST) and future test technologies through EDA tools. After this course, students can opt his/her career as test engineers in semiconductor technologies.

Course Outcome: After completion of the Course, Students will be able to:

No	Course Outcomes	RBT Level*
01	Appreciate the need of the design for testability.	UN
02	Apply the concept of design for testability.	AP
03	Compare different logic and fault simulation techniques.	AN
04	Apply the concept of BIST and its different architectures.	AP
05	Evaluate various ATPG algorithms.	EL

Course Scheme:

Teaching Scheme			**Total Credits**	**Assessment Pattern and Marks**				**Total Marks**
				Theory		**Practical**		
L	**T**	**PR**	**C**	**ESE (E)**	**PA(M)**	**ESE (V)**	**PA (I)**	
03	00	02	04	70	30	30	20	150

Course Content:

U. No	**Course Content**	**No of Hours**	**% weightage**
1	**Introduction:** Importance of testing, testing during the VLSI lifecycle, Challenges in VLSI testing, levels of abstraction in VLSI testing, historical review of VLSI test technology.	04	05

2	**Design for Testability:** Introduction, testability analysis, design for testability basics, scan architecture, scan design rules, special-purpose scan designs, RTL design for testability.	08	20
3	**Logic and Fault Simulation:** Introduction, simulation models: Gate-level network, logic symbols, logic element evaluation, timing models, Logic Simulation: compiled-code simulation, event-driven simulation, compiled-code Vs event-driven simulation, hazards, Fault simulation: serial fault simulation, parallel fault simulation, deductive fault simulation, concurrent fault simulation, differential fault simulation, fault detection, comparison of fault simulation techniques, alternatives to fault simulation.	08	20
4	**Test Generation:** Introduction, random test generation, theoretical background: Boolean difference, designing a Stuck-At ATPG for combinational circuits: A naïve ATPG algorithm, a basic ATPG algorithm, D algorithm, PODEM, FAN, static logic implication, dynamic logic implications, Designing a sequential ATPG: time frame expansion, 5-valued algebra Is insufficient, gated clocks and multiple clocks, Unstable faulty identification, Designing a simulation-based ATPG, Advanced simulation-based ATPG, hybrid deterministic and simulation-based ATPG, ATPG for Non-Stuck-At faults, other topics in Test Generation.	10	25
5	**Logic Built-In Self-Test:** Introduction, BIST design rules: unknown source blocking, re-timing, Test Pattern Generation: exhaustive testing, pseudo-random testing, pseudo-exhaustive testing, delay fault testing, Output Response Analysis: one count testing, transition count testing, signature analysis, Logic BIST Architectures: BIST architectures for circuits without scan chains, BIST architectures for circuits with scan chains, BIST architectures using register reconfiguration, modified Built-In logic block observer, concurrent Built-In logic block observer, CSTP, BIST architecture using concurring checking circuits: concurrent self-verification, Fault Coverage Enhancement: test point insertion, mixed-mode BIST, hybrid BIST, BIST Timing Control: single-capture, skewed-load, double-capture, fault detection, A Design Practice: BIST rule checking and violation repair, logic BIST system design, RTL BIST synthesis, design verification and faulty coverage,	12	30
		42	100

Reference Book:

- Laung-Terng Wang, Cheng-Wen Wu, Xiaoqing Wen, VLSI Test Principles and Architectures Design for Testability, Morgan Kaufmann Publishers, 2006.

- M. Abramovici, M. A. Breuer and A. D. Friedman, Digital Systems Testing and Testable Design, IEEE Press, 1990.
- M.Bushnell and V. D. Agrawal, Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers, 2000.

Suggested Course Practical List:

- The practical work will be carried out based on the content covered during the academic session.

List of Laboratory/Learning Resources Required:

- List of Hardware: FPGA/CPLD programming tool,
- List of Software: EDA Tools – Cadence, Synopsis, Siemens
- List of Useful websites MOOCs:---
    - Course-related online MOOCs on NPTEL/SWAYAM platform
    - Recent publications in reputed journal/conferences

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