GUJARAT TECHNOLOGICAL UNIVERSITY

Program Name: Master of Engineering
Level: PG
Branch: Electronics And Communication (VLSI Design)
Subject Code: ME02096031
Subject Name: Semiconductor Memory Circuits Design

WEF Academic Year	2025-26
Semester	02
Category of the Course	PEC-03

Prerequisite:	Basic analog and digital CMOS circuits
Rationale:	Currently, there are requirement of high speed, excellent performance and huge capacity of memory chips due to advances in computing technologies and AI/ML based systems. The student in the course learns contemporary concepts of various design methodologies of emerging volatile/nonvolatile memories, various fault models and testing procedures for semiconductor memories, and advanced memory technologies for future requirements.

Course Outcome:

After Completion of the Course, Student will be able to:

No	Course Outcomes	RBT Level*
01	Analyze operation of different SRAM and DRAM.	AN
02	Analyze operation of different non-volatile semiconductor memories.	AN
03	Model different memory faults.	AP
04	Analyze memory testing techniques.	AN
05	Evaluate advanced memory technologies.	EL

*RM: Remember, UN: Understand, AP: Apply, AN: Analyze, EL: Evaluate, CR: Create

Course Scheme:

Teaching Scheme			Total Credits	Assessment Pattern and Marks				Total Marks
				Theory		Practical		
L	T	PR	C	ESE (E)	PA(M)	ESE (V)	PA (I)	
03	00	02	00	70	30	30	20	150

Course Content:

U. No	Course Content	No of Hours	% weightage
1	**Random Access Memory Techniques:** Introduction, static random-access memories (SRAMs): SRAM (NMOS and CMOS cell structures, MOS SRAM architectures, MOS SRAM cell and peripheral circuit operation, bipolar SRAM technologies, Silicon-on-Insulator (SCI) technology, advanced SRAM architectures and technologies, application-specific SRAMS. Dynamic Random-Access Memories (DRAMs), DRAM technology development, CMOS DRAMs, DRAM cell theory and advanced cell structures, BiCMOS DRAMs, soft-error failures in DRAMS, advanced DRAM designs and architectures, a 16-Mb DRAM, ULSI DRAM developments. Application-Specific DRAMs: Pseudo static DRAMS, silicon file, video DRAMS, high-speed DRAMs, application-specific RAM glossary and summary.	10	25
2	**Nonvolatile Memories:** Introduction, Masked Read-Only memories (ROMs): technology development and cell programming, ROM cell structures, high-density ROMs. Programmable Read-Only memories (PROMs): bipolar PROMs, CMOS PROMs. Erasable -Programmable Read-Only Memories (EPROMs): floating-gate EPROM cell, EPROM technology developments, advanced EPROM architectures, OTP EPROMS. Electrical Erasable PROMS (EEPROMs): EEPROM technologies, EEPROM architectures, nonvolatile SRAM. Flash memories (EPROMs/EEPROMs): flash memory cells and technology developments, advanced flash memory architectures.	8	20
3	**Memory Fault Modeling and Testing:** Introduction, RAM fault modeling: stuck-at faulty model, bridging faults, coupling faults, pattern-sensitive faults, miscellaneous faults, GaAs SRAM fault modeling and testing, embedded DRAM faulty modeling and testing. RAM Electrical Testing: DC and AC parametric testing, functional testing and some commonly used algorithms, functional test pattern selection. RAM pseudorandom testing, megabit DRAM testing, nonvolatile memory modeling and testing: DC electrical measurements, AC and functional measurements. IDDQ fault modeling and testing, application specific memory testing.	8	20
4	**Memory Design for Testability and Faulty Tolerance:** general design for testability techniques: Ad Hoc design techniques, structured design techniques. RAM Built-In Self-Test (BIST): BIST using algorithmic test sequence, BIST using 13N March algorithm, BIST for pattern-sensitive faults, BIST using BILBO. Embedded memory DFT and BIST techniques, Advanced BIST and Built-In Self-Repair architectures, DFT and BIST for ROMs, memory error detection and correction techniques, memory fault-tolerance designs	10	25

5	**Advanced Memory Technologies:** Introduction, Ferroelectric RAMs (FRAMS): basic theory, FRAM cell and memory operation, FRAM technology developments, FRAM reliability issues, FRAM radiation effects, FRAMS Vs EEPROMs. GaAs FRAMS, analog memories, magnetoresistive RAMs (MRAMs), experimental memory devices: quantum-mechanical switch memories, a GaAs n-p-n-p Thyristor/JFET memory cell, single electron memory, neuron-MOS multiple-valued memory technology.	6	10
		42	100

Reference Book:

- Ashok K. Sharma, Advanced Semiconductor Memories: Architectures, Designs, and Applications, Wiley Interscience, 1997.
- Luecke Mize Care, “Semiconductor Memory design & application”, Mc-Graw Hill.

Suggested Course Practical List:

- The practical work will be carried out based on the content covered during the academic session.

List of Laboratory/Learning Resources Required:

- List of Hardware: FPGA/CPLD programming tool, Multimeter, Power supply, function generator, oscilloscope
- List of Software: EDA Tools – Cadence, Synopsis, Siemens
- List of Useful websites MOOCs:---
    - Course-related online MOOCs on NPTEL/SWAYAM platform
    - Recent publications in reputed journal/conferences

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