GUJARAT TECHNOLOGICAL UNIVERSITY

Program Name: Master of Engineering
Level: PG
Branch: Electronics And Communication (VLSI Design)
Subject Code: ME02096021
Subject Name: Low Power CMOS Circuits Design

WEF Academic Year	2025-26
Semester	02
Category of the Course	PEC 3

Prerequisite:	Fundamentals of MOS Transistor
Rationale:	In any computing system, there is a need for memory chips and circuits that have high speed, high performance and low power dissipation. This course covers various aspects regarding the design of low power CMOS circuits. The course includes issues related design of low power VLSI circuits, techniques for low-power VLSI circuit designs, advanced VLSI circuit designs, methodologies for low power combinational and sequential VLSI circuit designs. The students can design and develop low-power electronics systems for many applications after completion of the course.

Course Outcome:

After completion of the Course, Students will be able to:

No	Course Outcomes	RBT Level*
01	Analyze different power dissipation components in CMOS circuit design.	AN
02	Analyze scaling and short-channel effects in MOSFET device.	AN
03	Apply energy reduction techniques for the design of low power CMOS inverter design.	AP
04	Apply low power design techniques for CMOS combination and sequential circuits.	AP
05	Evaluate performance of various low power CMOS circuit design techniques.	EL

*RM: Remember, UN: Understand, AP: Apply, AN: Analyze, EL: Evaluate, CR: Create

Course Scheme:

Teaching Scheme			**Total Credits**	**Assessment Pattern and Marks**				**Total Marks**
				Theory		**Practical**		
L	**T**	**PR**	**C**	**ESE (E)**	**PA(M)**	**ESE (V)**	**PA (I)**	
03	00	02	04	70	30	30	20	150

Course Content:

U. No	Course Content	No of Hours	% weightage
1	**Introduction to Low Power Issues in VLSI :** Switching power consumption, short – circuit power consumption, leakage power consumption, low power IC design beyond Sub-20 nm Technology, issues related to silicon manufacturability and variation, issues related to design productivity, limitation faced by CMOS, international technology roadmap for semiconductors, different groups of MOSFETs, three MOS types, low leakage MOSFET, importance of subthreshold slope, why is subthreshold current exponential in nature?, subthreshold leakage and voltage limits, importance of subthreshold slope in low power operation, ultralow voltage operation, low power analog circuit design, fundamental consequence of lowering supply voltage, analog MOS transistor performance parameters.	6	10
2	**Scaling and Short Channel Effects in MOSFET :** MOSFET scaling, influence of voltage scaling on power and delay, VTCMOS circuits, MTCMOS circuits, gate oxide scaling, gate leakage current, mobility, high-k gate dielectrics, key guidelines for selecting an alternative gate Dielectric, materials, gate tunnelling current, gate length scaling, introduction to short channel effect in MOSFET, Reduction of Effective Threshold Voltage, Drain-induced Barrier Lowering, Mobility Degradation and Surface Scattering, Surface Scattering, Hot Carrier Effect, Punchthrough Effect, Velocity Saturation Effect, Increase in Off-state Leakage Current, Lightly Doped Drain Structure, Channel Engineering Technique, Gate Engineering Technique, Single Halo Dual Material Gate MOSFET, Double Halo Dual Material Gate MOSFET, Double Gate MOSFET, Dual Material Double Gate MOSFET, Triple Material Double Gate MOSFET, FinFET, Triple Gate MOSFET, Gate-all-around MOSFET, Surrounding Gate MOSFET, Silicon Nanowires, Fringing-induced Barrier Lowering, Silicon-on- insulator MOSFETs.	8	20
3	**Advanced Energy-reduced CMOS Inverter Design:** Introduction, Transfer Characteristics of Inverter, Static CMOS Inverter in Super- threshold Regime, Introduction to Subthreshold Logic.	8	20

4	**Advanced Combinational Circuit Design:** Static CMOS Logic Gate Design, Complementary Properties of CMOS Logic, Pseudo-nMOS Gates, Sizing of Transistor in CMOS Design Style, Introduction to Logical Effort, Delay Estimation by Logical Effort, Tristate Buffer, Transmission Gates and Tristate, Implementation of Combinational Circuit Using DTMOS Logic for Ultralow Power Application, ECLR Structure, Power Consumption, Propagation Delay.	10	25
5	**Advanced Energy-reduced Sequential Circuit Design:** Basics of Regenerative Circuits, Basic SR Flip-flop/Latch, Clocked JK Latch, Master–slave Flip-flop, D Latch, Master–slave Edge-triggered Flip-flops, Timing Parameters for Sequential Circuits, Clock Skews due to Non-ideal Clock Signal, Design and Analysis of the Flip-flops Using DTMOS Style, Adiabatic Flip-flop.	10	25
		42	100

Reference Book:

- Angsuman Sarkar, Swapnadip De, Manish Chanda, Chandan Kumar Sarkar, Low Power VLSI Design: Fundamentals, De Gruyter Oldenbourg Publisher, 2016
- Kiat-Seng Yeo, Kaushik Roy, Low-Voltage, Low-Power VLSI Systems, McGraw-Hill Education, 2004
- Kaushik Roy, Sharat Prasad, Low-Poer CMOS VLSI Circuit Design, Wiley, 2000.

Suggested Course Practical List:

- The practical work will be carried out based on the content covered during the academic sessions.

List of Laboratory/Learning Resources Required:

- List of Hardware: FPGA/CPLD programming tool, Multimeter, Power supply, function generator, oscilloscope
- List of Software: EDA Tools – Cadence, Synopsis, Siemens
- List of Useful websites MOOCs:---
- Course-related online MOOCs on NPTEL/SWAYAM platform
    - Recent publications in reputed journal/conferences

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