GUJARAT TECHNOLOGICAL UNIVERSITY

Programme Name: Master of Engineering
Level: PG
Branch: Electronics And Communication (Signal Processing & VLSI Technology)
Subject Code : ME02026011
Subject Name : VLSI Signal Processing

WEF Academic Year :	2024_25
Semester :	2
Category of the Course :	PCC-04

Prerequisite :	Basic subject on methodologies to design VLSI system for signal processing applications
Rationale :	Knowledge of basic CMOS circuit design

Course Outcome :

After Completion of the Course, Student will able to :

No	Course Outcomes	RBT Level*
01	Understand the concept and requirements of iteration bound	**UN**
02	Apply basics of pipelining and parallel processing to design the system for high speed and low power requirements.	**AP**
03	Perform folding, unfolding and retiming operations on the given systems	**AP**
04	Implement various algorithms based on systolic architectures.	**CR**
05	Evaluate bit level arithmetic and redundant arithmetic techniques.	**EL**

*RM: Remember, UN: Understand, AP: Apply, AN: Analyze, EL: Evaluate, CR: Create

Teaching and Examination Scheme :

Teaching Scheme			Total Credits	Assessment Pattern and Marks				Total Marks
				Theory		Practical		
L	T	PR	C	ESE (E)	PA(M)	ESE (V)	PA (I)	
3	0	2	4	70	30	30	20	150

Course Content :

Sr. No.	Course Content	No. of Hours	% of Weightage
1	**Introduction to DSP algorithms, Iteration bound:** Typical DSP algorithms: Convolution, Correlation, Digital-filters, adaptive filters etc. Data-flow graph representations, iteration bound and its computation, iteration bound of Multirate data-flow graphs.	10	20
2	**Pipelining, Parallel Processing and Retiming:** Pipelining of FIR filters, Parallel processing, Pipelining and Parallel Processing for low power, definitions and properties of retiming, system inequalities and its solution, retiming techniques.	8	25
3	**Unfolding and Folding**: Algorithm for unfolding, properties of unfolding, Comparative analysis of (i) critical path (ii) unfolding and (iii) retiming. Folding transformation, Register minimization techniques, folding of Multirate systems.	8	25
4	**Systolic Architecture Design:** Systolic array design methodology, FIR systolic arrays, Selection of scheduling vector, Matrix-matrix multiplication and 2D systolic array design, systolic design for space representations containing delays.	6	15
5	**Bit-Level Arithmetic Architecture and Redundant Arithmetic:** Parallel multipliers, Interleaved floor-plan and bit-plan based filters, Bit-serial multipliers, Bit-serial filter design and implementation, Canonic signed digit arithmetic, distributed arithmetic, Redundant number representations, Carry-free radix-2 addition and subtraction, Hybrid radix-4 addition, Hybrid redundant multiplication architectures, Data format converter.	10	15
	Total	**42**	**100**

Suggested Course Practical List :

1. Keshab K. Parhi, “VLSI Digital Signal Processing Systems”, Wiley, 2010.
2. Magdy A. Bayoumi, E. Swartzlander, “VLSI Signal Processing Technology”, Springer Science, 1994.
3. Peter B. Denyer, David Renshaw, “VLSI signal processing: a bit-serial approach”, Addison-
4. Wesley, 1985.

List of Laboratory/Learning Resources Required :

1. Compute the iteration bound for the given data flow graph (DFG).
2. Determine the iteration bound for the given multi rate DFG.
3. For given DFG place pipelining register at appropriate places to achieve required sample rate.
4. For given DFG calculate critical path and place pipelining latches to reduce critical paths.
5. For given DFG place pipeline structure to reduce power consumption.
6. Design a given FIR filter with pipeline and parallel processing for power reduction and sampling rate improvement.
7. For given DFG apply retiming techniques to minimize the clock period.
8. Solve the problem of critical path using unfolding techniques for given DFG.
9. Design the folded architecture for the 6-tap FIR filter.
10. Design systolic-architecture for matrix-vector multiplication.
11. Design bit-parallel architecture for six-bit addition.
12. Design a MSD-first radix-4 maximally redundant to non-redundant converter for word length of 8 digits.

List of Open Source Software/learning website:

1. www.nptel.ac.in
2. www.ocw.mit.edu

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