GUJARAT TECHNOLOGICAL UNIVERSITY

Program Name: Master of Engineering

Level: PG

Subject Code: ME02000961

Subject Name : Memory Technology

WEF Academic Year :	2024-25
Semester :	2
Category of the Course :	Professional Elective Course

Prerequisite :	Basic knowledge of Microelectronic Devices and VLSI Circuit Design.
Rationale :	For the modern and futuristic era of artificial intelligence and machine learning based computing systems, memory chips/circuits with extremely high speed/performance and capacity are the utmost requirements. This course provides a platform for students to understand the contemporary memory technology designs and their limitations. This course also provides an overlook on the emerging volatile/nonvolatile memory technologies which are prominent contenders for becoming the part of futuristic computing framework. This course provides an identification of various fault models, modes and mechanisms in semiconductor memories and their testing procedures..

Course Outcome :

After Completion of the Course, Student will be able to :

No	Course Outcomes	RBT Level*
1	Analyze and Design SRAMs and DRAMs.	AN
2	Analyze the operations of a semiconductor memory bit-cell and its related stability, variabilityand reliability issues.	AN
3	Understand and analyze the NVMs.	UN
4	Understand the industry trend of the emerging memory technologies and able to compare them with the contemporary memory architectures.	UN
5	Identify various fault models, modes and mechanisms in semiconductor memories and theirtesting procedures.	UN

*RM: Remember, UN: Understand, AP: Apply, AN: Analyze, EL: Evaluate, CR: Create

Course Scheme :

Teaching Scheme			Total Credits	Assessment Pattern and Marks				Total Marks
				Theory		Practical		
L	T	PR	C	ESE (E)	PA(M)	ESE (V)	PA (I)	
4	0	0	4	70	30	0	0	100

Course Content :

Sr. No.	Course Content	No. of Hours	% of Weightage
1	**Introduction : Overview of memory technologies, Memory organization, market, trends and technologies.**	4	5
	Mainstream Semiconductor Memory Technologies :		
	A. Volatile Memories :		
2	Static Random Access Memory (SRAM) : SRAM Cell Structures, MOS SRAM Architecture, 6-T MOS SRAM Cell, CMOS SRAM Cell Design Strategy, Noise margin, Stability, Scaling issues Read and Write circuitry, Sense amplifier, Advanced SRAMArchitectures, Application Specific SRAMs.	9	25
3	Dynamic Random Access Memory (DRAM) : 3-T DRAM operation, Read-Write Circuits, 1T-1C DRAM Cell Fabrication technology and capacitor structure, Soft Error Failures in DRAMsAdvanced DRAM Designs and Architecture-Application Specific DRAMs.	8	20
	B. Non-volatile Memories :		
4	Masked ROMs, CMOS PROM, EEPROMs, Floating Gate EPROM Cell, EEPROMs. Flash Memories: NAND v/s NOR architecture, Reliability, Scaling, and Multi-Level Cell capability (MLC), Advanced Flash Memory Architectures	8	15
	Emerging Memory Technologies :		
5	Resistive RAM (RRAM), Phase Change Memory (PCM), Ferroelectric RAM (FeRAM), Conductive Bridge RAM (CBRAM), Magneto-resistive RAMs: Spin-Transfer Torque MRAM (STT-MRAM) and Spin-Orbit Torque MRAM (SOT-MRAM), Comparative analysis of all eNVMs, Unconventional Applications of eNVMs: Neuromorphic Computing, Computing-inMemory (CiM). Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, High Density Memory Packaging	9	25
	Memory Fault Modeling and Design for Testability : RAM Fault Modeling, Electrical Testing, Pseudo Random Testing, Megabit DRAM Testing, Nonvolatile Memory Modeling and Testing, IDDQ Fault Modeling and Testing, Memory Built-In Self -Test (MBIST)	7	10
	Total	**45**	**100**

Reference Book :

1. Ashok K Sharma, “Advanced Semiconductor Memories: Architectures,Designs and Applications”, Wiley Interscience.

2. Ashok K. Sharma, “Semiconductor Memories: Technology, Testing and Reliability",Prentice-Hall of India Private Limited.
3. KiyooItoh, “VLSI memory chip design”, Springer International Edition.
4. Luecke Mize Care, “ Semiconductor Memory design & application”, Mc-Graw Hill.
5. CMOS Digital Integrated circuits – Analysis and Design by Sung – Mo Kang, Yusuf Leblebici,TATA McGraw-Hill Pub. Company Ltd.
6. Belty Prince, “ Semiconductor Memory Design Handbook”
7. Y. Nishi and Magyari-Kope, “Advances in non-volatile memory and storage technology,” Woodhead Publishing, 2019.
8. Roberto Gastaldi and Giovanni Campardo, “In Search of the Next Memory: Inside the Circuitry from the Oldest to the Emerging Non-Volatile Memories”, Springer, 2017.
9. Alberto Bosio, Luigi Dilillo, Patrick Girard, Serge Pravossoudovitch, Arnaud Virazel, “Advanced Test Methods for SRAMs: Effective Solutions for Dynamic Fault Detection in Nanoscaled Technologies,” Springer, 2010.
10. De Hao Yu and YuhaoWang, “Design Exploration of Emerging Nano-scale Non-volatile Memory,” Springer, 2014.

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