



GUJARAT TECHNOLOGICAL UNIVERSITY

Programme Name: Master of Engineering

Level: PG

Subject Code : ME02000171

Subject Name : VLSI Design Automation Algorithms

WEF Academic Year :	2024-25
Semester :	2
Category of the Course :	PEC-03

Prerequisite :	Basic knowledge of VLSI Chip Design and Graph Theory.
Rationale :	This course provides a platform for students to apply basic knowledge of algorithm to understand and implement complex physical design algorithms such as Circuit Partitioning, Floor planning, Placement, Grid and Global routing etc. This course gives insight into designing of various CAD Tools.

Course Outcome :

After Completion of the Course, Student will able to :

No	Course Outcomes	RBT Level*
01	Understand the concept of circuit partitioning and minimize the number of net crossing	UN
02	Determine the aspect ratio of each module to reduce the overall chip area	UN
03	Apply different algorithms to place the circuit components on layout surface to reduce the size of chip	AP
04	Understand different routing algorithms to minimize the overall wire length	UN
05	Learn the generation of optimize layout for different architectures	EL

*RM: Remember, UN: Understand, AP: Apply, AN: Analyze, EL: Evaluate, CR: Create

Teaching and Examination Scheme :

Teaching Scheme			Total Credits	Assessment Pattern and Marks				Total Marks
L	T	PR	C	Theory		Practical		
				ESE (E)	PA(M)	ESE (V)	PA (I)	
3	0	2	4	70	30	30	20	150



GUJARAT TECHNOLOGICAL UNIVERSITY

Programme Name: Master of Engineering

Level: PG

Subject Code : ME02000171

Subject Name : VLSI Design Automation Algorithms

Course Content :

Sr. No.	Course Content	No. of Hours	% of Weightage
1	Introduction : VLSI Design Process, Layout Styles, Difficulties in Physical Design, Definitions and Notation.	6	12
2	Circuit Partitioning : Introduction, Problem Definition, Cost Function and Constraints, Approaches to Partitioning Problem, Other Approaches and Recent Work	6	12
3	Floor planning : Introduction, Problem Definition, Approaches to Floor planning, Other Approaches and Recent Work.	6	12
4	Placement : Introduction, Problem Definition, Cost Functions and Constraints, Approaches to Placement, Other Approaches and Recent Work.	6	12
5	Grid Routing : Introduction, Problem Definition, Cost Functions and Constraints, Maze Routing Algorithms, Line Search Algorithms, Other Issues, Other Approaches and Recent Work.	6	12
6	Global Routing : Introduction, Cost Functions and Constraints, Routing Regions, Sequential Global Routing, Integer Programming, Global Routing by Simulated Annealing, Hierarchical Global Routing, Other Approaches and Recent Work.	6	12
7	Channel Routing : Introduction, Problem Definition, Cost Functions and Constraints, Approaches to Channel Routing, Other Approaches and Recent Work.	5	12
8	Layout Generation : Introduction, Layout Generation, Standard-cell Generation, Optimization of Gate-matrix Layout, Programmable Logic Arrays, Other Approaches and Recent Work.	7	16
	Total	48	100

Reference Book :

1. VLSI Physical Design Automation, Theory and Practice, Sadiq M. Sait and Habib Youssef. By world scientific press.
2. Algorithm for VLSI physical design automation by Sherwani and navneed- by Springer /B S Publication (2008).
3. N. Sherwani, Algorithms for VLSI Physical Automation, Third Edition, Kluwer, 1998.
4. S. H. Gerez, Algorithms for VLSI Design Automation, Wiley, 1998.
5. A. Micozo, Digital Logic Testing and Simulation, Second edition, Wiley, 2003.
6. S. M. Sait and H. Yousuf, Iterative Computer Algorithm with Applications in Engineering, Wiley/IEEE, 2002.



GUJARAT TECHNOLOGICAL UNIVERSITY

Programme Name: Master of Engineering

Level: PG

Subject Code : ME02000171

Subject Name : VLSI Design Automation Algorithms

7. C. Visweswariah and S. Duvall, Computer Aided Optimization of Digital Integrated Circuits, Wiley, 2002.
8. G. De Micheli, Synthesis and Optimization of Digital Circuits, Mcgraw-Hill International, 1994

Suggested Course Practical List :

1. Introduction to Various CAD Design Tools and its comparisons.
2. Implementation of Dijkstra's routing algorithm.
3. Implementation of the Kernighan Lin Algorithm for circuit partitioning.
4. Implementation of the Fiduccia Mattheyses Algorithm for circuit partitioning
5. Implementation of the Simulated Annealing Algorithm.
6. Implementation of the Genetic Algorithm.
7. Implementation of Yoshimura and Kuh algorithm.
8. Implementation of the Linear Ordering Cluster Growth Algorithm.
9. Implementation of the Unconstrained Algorithm for channel routing.
10. Implementation of the vertical constrained Algorithm for channel routing.
11. Seminar report for a given research topic.
12. Case study: Modification in any existing algorithm.
13. Minor project

List of Laboratory/Learning Resources Required :

SciLAB / MATLAB

1. <http://wwwhome.ewi.utwente.nl/~gerezsh/cadvlsi/book.html>
2. <http://www.personal.kent.edu/~rmuhamma/GraphTheory/graphTheory.htm>
3. <http://compprog.wordpress.com/2007/11/09/minimal-spanning-trees-prim-s-algorithm/>
4. <http://www.people.vcu.edu/~gasmerom/MAT131/mst.html>
5. <http://www.personal.kent.edu/~rmuhamma/GraphTheory/MyGraphTheory/trees.htm>
6. <http://graphics.stanford.edu/courses/cs448b-02-winter/lectures/treesgraphs/tree.graph.pdf>
7. <http://www.slideshare.net/purpleinkredshirt/introduction-to-graph-theory>
8. <http://lecturesppt.blogspot.in/2011/09/graphs-and-algorithms-pdf-ppt-slides.html>
9. <http://www.authorstream.com/Presentation/ankush85-159135-nphard-nphard171-175-education-ppt-powerpoint/>
10. <http://www.authorstream.com/Presentation/nitinmishra10-83453-complexity-algorithmdatastructure-algorithms-lecture-3-education-ppt-power>

* * * * *