



GUJARAT TECHNOLOGICAL UNIVERSITY

Program Name: Master of Engineering

Level: PG

Branch: Electronics and Communication (VLSI Design)

Subject Code: ME01096061

Subject Name: Logic Design using FPGA

WEF Academic Year	: 2025-26
Semester	: 01
Category of the Course	: PEC-02

Prerequisite:	Digital Electronics fundamentals, mathematics
Rationale:	This course provides a platform for students to apply basic knowledge of digital electronics, design of digital circuits on FGPA boards using Verilog/VHD.L. Various combinational and sequential digital circuits are analyzed using FPGA boards and able to understand and implement complex digital circuit design. This course gives insight into designing of various digital blocks on FPGA boards.

Course Scheme:

Teaching Scheme			Total Credits	Assessment Pattern and Marks				Total Marks
L	T	PR	C	Theory		Practical		
				ESE (E)	PA(M)	ESE (V)	PA (I)	
03	00	02	04	70	30	30	20	150

Course Content:

U. No	Course Content	No of Hours	% of Weightage
1	Field-Programmable Gate Arrays: Introduction, FPGA building blocks: layout of Xilinx FGPA, input/out blocks, configurable logic blocks, interconnect resources, block RAM, DSP slices, clock management, the XADC block, high-speed serial I/O transceivers, peripheral component interconnect express interface, FPGA-based digital system design philosophy, usage areas of FPGAs	6	15



GUJARAT TECHNOLOGICAL UNIVERSITY

Program Name: Master of Engineering

Level: PG

Branch: Electronics and Communication (VLSI Design)

Subject Code: ME01096061

Subject Name: Logic Design using FPGA

2	The Vivado Design suite: Installation, creating a new project, synthesizing the project, simulation the project, implementing the synthesized project, programming the FPGA, Vivado design suit IP management, application on the Vivado design suite	6	15
3	Introduction to Verilog and VHDL: Verilog fundamentals, testbench formation in Verilog, VHDL fundamentals, testbench formation in VHDL, adding an existing IP to the project.	4	10
4	Data Types and Operation: Number representations, negative numbers, fixed- and floating-point representation, ASCII code, arithmetic operations on binary numbers, data types in Verilog, operation in Verilog, data types in VHDL, application on data types and operators, application on data types and operators, FPGA building blocks used in data types and operators	4	10
5	Combinational Circuits: combinational circuit analysis, combinational circuit implementation, combinational circuit design, sample designs, applications on combinational circuits, FPGA building blocks used in combinational circuits.	4	05
6	Combinational Circuit blocks: Adders, comparators, decoders, encoders, multiplexers, parity generators and checkers, applications on combinational circuit blocks, FPGA building blocks used in combinational circuit blocks.	6	15
7	Data Storage Elements: Latches, flip-flops, registers, memory, read-only memory, random access memory, application on data storage elements, FPGA building blocks used in data storage elements	6	15
8	Sequential Circuits: sequential circuit analysis, timing in sequential circuits, shift register as a sequential circuit, counter as a sequential circuit, sequential circuit design, application on sequential circuits, FPGA building blocks used in sequential circuits.	6	15
		42	100

Reference Book:

- Digital System Design with FPGA – Implementation Using Verilog and VHDL, Cem Unsahn, Bora Tar, McGraw Hill Education, 2017.



GUJARAT TECHNOLOGICAL UNIVERSITY

Program Name: Master of Engineering

Level: PG

Branch: Electronics and Communication (VLSI Design)

Subject Code: ME01096061

Subject Name: Logic Design using FPGA

- Digital Logic: With an Introduction to Verilog and FPGA-Based Design, M. Rafiquzzaman, Steven A. McNinch, 1st Edition, Wiley Publication, 2020
- Advanced Digital Logic Design using VHDL, State Machines, and Synthesis for FPGA, Sunggu Lee, CL Engineering, 2005

Course Outcome:

After completion of the Course, Students will be able to:

No	Course Outcomes	RBT Level*
01	Understand various blocks of FPGA, the Vivado design suite, Verilog and VHDL	UN
02	Design combinational circuits and block using Verilog/VHDL on FPGA boards	AP
03	Design sequential circuits and blocks using Verilog/VHDL on FPGA boards	AP
04	Design of data storage circuit elements on FPGA boards	AP
05	Measure performance parameters of circuits realized on FPGA boards.	AP

*RM: Remember, UN: Understand, AP: Apply, AN: Analyze, EL: Evaluate, CR: Create

Suggested Course Practical List:

- The practical work will be carried out based on the content covered during the academic session.

List of Laboratory/Learning Resources Required:

- List of Hardware: FPGA/CPLD programming tool,
- List of Software: EDA Tools – Cadence, Synopsis, Siemens
- List of Useful websites MOOCs:---
 - Course-related online MOOCs on NPTEL/SWAYAM platform
 - Recent publications in reputed journal/conferences
