GUJARAT TECHNOLOGICAL UNIVERSITY

Program Name: Master of Engineering
Level: PG
Branch: Electronics And Communication (VLSI Design)
Subject Code: ME01096021
Subject Name: VLSI Technology

WEF Academic Year	2025-26
Semester	01
Course Name & Code	PCC-02

Prerequisite:	VLSI fabrication technology, manufacturing of VLSI devices, Basics of semiconductor physics
Rationale:	Students must possess a good understanding of semiconductor chip fabrication process. Students must learn in detail about various processing steps utilized in fabrication of semiconductor chips. As well student should possess knowledge of various analytical and assembly techniques. Student should be familiar with yield and reliability issue in VLSI.

Course Scheme:

Teaching Scheme			Total Credits	Assessment Pattern and Marks				Total Marks
				Theory		Practical		
L	T	PR	C	ESE (E)	PA(M)	ESE (V)	PA (I)	
03	00	02	04	70	30	30	20	150

Course Content:

U. No	Course Content	No of Hours	% of Weightage
1	**Crystal Growth, Wafer Preparation, Epitaxy and Oxidation**: Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing considerations and future trends, Vapor phase Epitaxy, Molecular Beam Epitaxy, Silicon on Insulators, Epitaxial Evaluation and future trends, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxide properties, Redistribution of Dopants at interface, Oxidation of Poly Silicon,	10	25

	Oxidation inducted Defects.		
2	**Lithography and Relative Plasma Etching:** Optical Lithography, Electron Lithography, X-Ray Lithography, Ion Lithography, Plasma properties, Feature Size control and Anisotropic Etch mechanism, Reactive Plasma Etching techniques and Equipment, Specific etch processes and future trends.	10	25
3	**Deposition, Diffusion, Ion Implantation and Metallization:** Deposition process, Poly silicon, plasma assisted Deposition, Models of Diffusion in Solids, Fick's one dimensional Diffusion Equations, Atomic Diffusion Mechanism, Measurement techniques, Range theory, Implant equipment. Annealing Shallow junctions, High-energy implantation, Physical vapor deposition, Patterning and future trends	10	25
4	**Process Simulation and VLSI Process Integration:** Ion implantation, Diffusion and oxidation, Epitaxy, Lithography, Etching and Deposition, NMOS IC Technology, CMOS IC Technology, MOS Memory IC technology, Bipolar IC Technology, IC Fabrication and future trends.	12	25
		42	100

Reference Book:

- S. M. Sze, "VLSI Technology", McGraw Hill Second Edition. 1998.
- S.K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc., New York, 1983
- James D Plummer, Michael D. Deal, Peter B. Griffin, "Silicon VLSI Technology:
- Fundamentals Practice and Modeling", Prentice Hall India.2000.

Course Outcome:

After completion of the Course, Students will be able to:

No	Course Outcomes	RBT Level*
01	Understand semiconductor fabrication processes.	UN
02	Identify challenges with various semiconductor fabrication processes.	AN

03	Simulate various semiconductor fabrication processes.	AP
04	Observe effect of control parameters involved in various semiconductor fabrication processes.	AN
05	Model steps involved in semiconductor fabrication processes.	AP

*RM: Remember, UN: Understand, AP: Apply, AN: Analyze, EL: Evaluate, CR: Create

Suggested Course Practical List:

- The practical work will be carried out based on the content covered during the academic sessions.

List of Laboratory/Learning Resources Required:

- List of Hardware: FPGA Boards
- List of Software/Open Source Tools/Simulator: ANSYS EDA Tools
- List of Useful websites/MOOCs
  - Course-related online MOOCs on NPTEL/SWAYAM platform
  - Recent publications in reputed journal/conferences

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