



# GUJARAT TECHNOLOGICAL UNIVERSITY

**Program Name: Master of Engineering**

**Level: PG**

**Branch: Electronics & Communication (VLSI System Design)**

**Course / Subject Code : ME01000411**

**Course / Subject Name : VLSI Design Verification**

WEF Academic Year :	2024 – 25
Semester :	1 <sup>st</sup> Semester
Category of the Course :	PEC

**Type of course:** Analysis and Design of CMOS based Digital Circuits

<b>Prerequisite :</b>	Basic Digital Electronics and CMOS based circuits.
<b>Rationale:</b>	This course will provide an opportunity to the students to learn about various topics of VLSI such as design of digital circuits using MOSFET device as well as using hardware description language (HDL). In laboratory part of this course, students will be given exposure to HDL for automated design of digital circuits. This subject is very important for the students who would like to pursue their career in VLSI domain.

**Course Scheme:**

Teaching Scheme			Total Credits	Assessment Pattern and Marks				Total Marks
L	T	PR	C	Theory		Practical		
				ESE (E)	PA(M)	ESE (V)	PA (I)	
3	0	2	4	70	30	30	20	150

**Course Content:**

Sr. No.	Course Content	No. of Hours	% of Weightage
1	<b>The Verification Plan</b> The Role of the Verification Plan, Levels of Verification, Verification Strategies, From Specification to Features, From Features to test cases, From Test cases to Test benches.	5	10
2	<b>Verification Tools</b> Linting Tools, Simulators, Third-Party Models, Waveform Viewers, Code Coverage, Verification Languages, Revision Control, Issue Tracking, and Metrics.	6	15



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3	<b>Functional Verification Methods and Tools</b> Concept, Test bench architecture, Simulation tools, Functional and code coverage	6	15
4	<b>Formal Verification Methods</b> Binary Decision Diagram, Equivalence Checking, Assertion based verification, Emulation	6	15
5	<b>Introduction to System Verilog</b> System Verilog modeling concepts, Data types, declarations, syntax rules, Procedural blocks and assignments, Programming statements, Operators and operation rules, Compound data types and packages, System Verilog interface ports, Verification constructs and test bench interfaces, Verification timing using clocking blocks, Object Oriented test bench, Dynamic arrays and scoreboards, Constrained random stimulus generation, Functional coverage, Synchronization (events, mailboxes, emaphores), Assertions overview	10	25
6	<b>Universal Verification Methodology (UVM)</b> Introduction, Overview of UVM, Object Oriented Programming, UVM library Basics, Interface Universal Verification Component	12	20
<b>Total</b>		<b>45</b>	<b>100</b>

## Reference Books:

1. Introduction to Formal Hardware Verification, T.Kropf, Springer Verlag, 2000
2. System-on-a-Chip Verification- Methodology and Techniques, P. Rashinkar, Paterson and L. Singh, Kluwer Academic Publishers, 2001
3. Janick Bergeron, "Writing test benches functional verification of HDL models" Kluwer Academic Publishers, New York, Boston, Dordrecht, London, Moscow, 2002.
4. Janick Bergeron, Writing Testbenches using SystemVerilog, Springer
5. Srikanth Vijayaraghavan, Meyyappan Ramanathan - A Practical Guide for System Verilog Assertions- Springer
6. Ray Salemi - The UVM Primer\_ An Introduction to the Universal Verification Methodology- Boston Light Press
7. Spear, Chris, Tumbush, Greg ,System Verilog for Verification- A guide to learning the test bench language features, Springer

## Course Outcome:

CO1: to help the engineers to design the system with Hardware Description Language and system Verilog  
CO2: to practice for writing synthesizable RTL models that work correctly in both simulation and Synthesis.

CO3: understand the features and capabilities of the UVM class library for system Verilog

CO4: combine multiple UVCs into a complete verification environment



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CO5: create and configure reusable, scalable, and robust UVM verification components (UVCs)

## **Suggested List of Experiments:**

- 1) Introduction to Verilog and System Verilog
- 2) Running simulator and debug tools
- 3) Experiment with 2 state and 4 state data types
- 4) Implementation of counters and testing.
- 5) Implementation of Mealy and Moore FSM and testing.
- 6) Experiment with blocking and non-blocking assignments
- 7) Model and verify simple ALU
- 8) Model and verify an Instruction stack
- 9) Use an interface between test bench and DUT
- 10) Developing a test program
- 11) Create a simple and advanced OO test bench
- 12) Use mailboxes for verification
- 13) Generate constrained random test values
- 14) Using coverage with constrained random tests
- 15) Simulate a simple UVM test bench and DUT
- 16) Examining the UVM test bench
- 17) Design and simulate sequence items and sequence
- 18) Design and simulate a UVM driver and sequencer
- 19) Design and simulating UVM monitor and agent
- 20) Design, simulate and examine coverage
- 21) Design and simulate a configurable UVM test environment

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