GUJARAT TECHNOLOGICAL UNIVERSITY

Program Name: Master of Engineering

Level: PG

Branch: Electronics & Communication (VLSI System Design)

Course / Subject Code :ME01000391

Course / Subject Name : VLSI Physical Design

w. e. f. Academic Year:	2024-25
Semester:	1st Semester
Category of the Course:	PEC

Prerequisite:	Basic implantation of various Algorithms.
Rationale:	The students need to learn basic concepts of VLSI physical design. The students will learn the floor planning and Pin allocations for the VLSI design. The students need to know the basic implementation of Algorithms for the placement and routing. The students will learn the design of various basic of timing analysis and clock tree synthesis.

Course Outcome:

After Completion of the Course, Student will able to:

No	Course Outcomes	RBT Level
01	Design and analyze different concepts of graph theory.	C
02	Understand basic principle, operation and applications of floor planning and pin allocation.	U
03	Comprehend and apply various algorithms to circuit partitioning Floor planning, Placement and Routing.	A
04	Study, analyze and implement the VLSI physical design using CAD tools.	C

**Revised Bloom's Taxonomy (RBT)*

Teaching and Examination Scheme:

Teaching Scheme (in Hours)			Total Credits L+T+ (PR/2)	Assessment Pattern and Marks				Total Marks
				Theory		Tutorial / Practical		
L	T	PR	C	ESE (E)	PA / CA (M)	PA/CA (I)	ESE (V)	
3	0	2	4	70	30	20	30	150

Course Content:

Unit No.	Content	No. of Hours	% of Weightage
1.	**Introduction to Graph Theory**: Dependency/ Constraint graphs, Steiner Tree, Cliques, Clustering and Spanning Tree	5	10
2.	**Circuit Level Partitioning**: Cost function and constrains, Algorithm for Circuit partitioning.	10	20
3.	**Floor planning and Pin Allocation**: Floor planning and pin allocation, Problem definition and cost functions.	12	30
4.	**Placement and Routing**: Placement and routing Algorithms, cost function and constrains, Area routing, Design Rule Check issue.	08	20
5.	**Clock Networks** : Basic concepts in clock networks, modern clock tree synthesis	05	05
6.	**Timing Analysis**: Timing closure, Timing Analysis and Performance constrains, Timing driven placement and routing, Physical synthesis.	05	15
	Total	**45**	**100**

Suggested Specification Table with Marks (Theory):

Distribution of Theory Marks (in %)					
R Level	**U Level**	**A Level**	**N Level**	**E Level**	**C Level**
10	**20**	**20**	**30**	**10**	**10**

Where R: Remember; U: Understanding; A: Application, N: Analyze and E: Evaluate C: Create (as per Revised Bloom's Taxonomy)

References/Suggested Learning Resources:

(a) Books:

1. Sadiq M Sait, Habib Youssef, and VLSI Physical Design Automation: Theory and Practice Publication: World Scientific.
2. Andrew B Kahng, Jens Lienig VLSI Physical Design: From Graph partitioning to Timing Closure, Publication: Springer.
3. Sung Kyu Lim , Practical Problems in VLSI Physical Design Automation, 2008 edition, Springer.

(b) Open source software and website:

1. https://nptel.ac.in/
2. VLSI physical design using CAD tools.

Suggested Course Practical List:

1. Simulation of graph theory for VLSI physical Design using MATLAB.
2. Simulation of Kernighan–Lin (KL) partitioning algorithm using MATLAB.
3. Simulation of Simulated annealing algorithm using MATLAB.
4. Synthesis and simulation of VLSI Design using cadence encounter/Magic/Proton.
5. Perform Floor-planning of VLSI design Cell using ILP solver for Integer Linear Programming.
6. Perform Placement of VLSI design using standard cells.
7. Perform Routing of VLSI design using standard cells.
8. Perform Static Timing Analysis for given logic diagram.
9. Perform zero stack algorithm for given logic diagram.
10. Implement small project on VLSI Physical Design.

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