GUJARAT TECHNOLOGICAL UNIVERSITY

Program Name: Engineering
Level: PG
Branch: Power Electronics
Course / Subject Code: ME01000291

Course / Subject Name: Semiconductor Technology

w. e. f. Academic Year:	2024-25
Semester:	1st Semester
Category of the Course:	PEC

Prerequisite:	NA
Rationale:	This course will provide an opportunity for the students to learn about various topics of Semiconductor Technology such as design of digital circuits using MOSFET device as well as VLSI Process Integration. This subject is very important for the students who would like to pursue their career in VLSI domain.

Course Outcome:

After Completion of the Course, the student will able to:

No	Course Outcomes
01	Understand the MOSFET device and its fabrication.
02	Learn various steps/procedures involved in chip design.
03	Understand the Concept of VLSI Process Integration.
04	Study latest developments in semiconductor technology.

Teaching and Examination Scheme:

Teaching Scheme in Hours)			Total Credits L+T+ (PR/2)	Assessment Pattern and Marks				Total Marks
				Theory		Tutorial / Practical		
L	T	PR	C	ESE (E)	PA / CA (M)	PA/CA (I)	ESE (V)	
3	0	2	4	70	30	20	30	150

Course Content:

Unit No.	Content	No. of Hours	% of Weightag

1.	**Introduction** Overview of VLSI design methodology, VLSI design flow, Design hierarchy, Concept of Regularity, Modularity, and Locality, VLSI design style, Design quality, package technology, Introduction to FPGA and CPLD, Computer Aided design technology, PLA, PAL, SPLD, ASIC, SoC Technology.	6	15%
2.	**MOS Transistor and its Fabrication** The Metal Oxide Semiconductor (MOS) structure, Structure and Operation of MOS transistor, MOSFET scaling, MOSFET capacitances Fabrication of MOSFET: Introduction, Basic steps, C-MOS n-Well Process. Layout Design rules, full custom mask layout design.	10	20%
3.	**Crystal Growth, Wafer Preparation, Epitaxy and Oxidation:** Electronic Grade Silicon, Czochralski crystal growing, Silicon Shaping, processing considerations and future trends, Vapor phase Epitaxy, Epitaxial Evaluation and future trends, Growth Mechanism and kinetics, Thin Oxides, Oxidation Techniques and Systems, Oxidation of Poly Silicon.	8	20%
4.	**Lithography and Relative Plasma Etching:** Optical Lithography, Electron Lithography, Feature Size control& Anisotropic Etch mechanism, Reactive Plasma Etching techniques and Equipment.	5	15%
5.	**Deposition, Diffusion, Ion Implementation and Metallization:** Deposition process, Poly silicon, plasma assisted Deposition. Atomic Diffusion Mechanism. Implant equipment, Annealing Shallow junctions, High-energy implantation. Physical vapor deposition, Patterning and future trends.	6	15%
6.	**Concept of VLSI Process Integration and Fin-FET Device:** Ion implantation, Diffusion and oxidation, Epitaxy, Lithography, Etching and Deposition, NMOS IC Technology, CMOS IC Technology, MOS Memory IC technology. FinFET Device: Introduction, need of FinFET device, Structure, working, Types, Comparison between FinFET and Planar MOSFET	7	15%
	Total	42	**100**

Suggested Specification Table with Marks (Theory):

Distribution of Theory Marks (%)					
R Level	U Level	A Level	N Level	E Level	C Level
40	20	20	10	10	0

Where R: Remember; U: Understanding; A: Application, N: Analyze and E: Evaluate C: Create (as per Revised Bloom's Taxonomy)

References/Suggested Learning Resources:

(a) Books:

1. CMOS Digital Integrated circuits – Analysis and Design by Sung – Mo Kang, Yusuf Leblebici, Tata McGraw-Hill Pub. Ltd.
2. S. M. Sze, "VLSI Technology", McGraw Hill Second Edition.
3. S.K. Ghandhi, VLSI Fabrication Principles, John Wiley Inc., New York,
4. Debprasad Das, "VLSI Design", Oxford University Press, Second Edition
5. W. R. Runyan, "Silicon Semiconductor Technology", Tata McGraw-Hill Pub. Ltd.
6. Fundamentals of Digital Logic Design with VHDL, Brown and Vranesic, McGraw-Hill Pub. Ltd.

(b) Open-source software and website:

1. https://nptel.ac.in/
2. https://www.design-reuse.com/articles/41330/cmos-soi-finfet-technology-review-paper.html

Suggested Course Practical List:

1. To study steps involved in VLSI design methodology.
2. Simulation of CMOS Inverter using SPICE for transfer characteristic.
3. To measure IDS – VGS and IDS – VDS characteristics for n-channel and p-channel MOSFETs.
4. To generate layout for CMOS Inverter circuit and simulate it for verification.
5. To measure propagation delay of a given CMOS Inverter circuit.
6. Simulation of CMOS Inverter using SPICE for transfer characteristic.
7. Introduction to programmable devices (FPGA, CPLD), Hardware Description Language (VHDL).
8. Implementation of basic logic gates and its testing.
9. Implementation of adder circuits and its testing.
10. Implementation 4 to 1 multiplexer /3 to 8 decoder and its testing.

11. Implementation of 8 to 3 priority encoder and its testing.
12. Implementation of J-K and D Flip Flops and its testing.
13. Implementation of sequential adder and its testing.
14. Implementation of BCD counter and its testing.
15. To study VLSI process Integration.
16. To study the FinFET Device.

List of Laboratory/Learning Resources Required:

VHDL – Programming tool, Circuit simulator,

FPGA/CPLD programming tool.

Suggested Activities for Students: If any

Students can be given case study / presentation based on various topics covered in theory.

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