



GUJARAT TECHNOLOGICAL UNIVERSITY

Program Name: Bachelor of Engineering

Level: UG

Subject Code : BE03041011

Subject Name : Digital Electronics

w. e. f. Academic Year:	2024-25
Semester:	3
Category of the Course:	PCC

Prerequisite:	NA
Rationale:	Understanding of principle, operation and analysis of digital electronics

Course Outcomes:

Sr. No.	CO statement	Marks % weightage
CO-1	Apply knowledge of Boolean algebra and other minimization techniques for digital circuit design.	20
CO-2	Identify, formulate and solve a problem based on combinational and sequential circuits	15
CO-3	Select the appropriate hardware and software tools for combinational and sequential circuit design.	20
CO-4	Comprehend the digital logic families.	15
CO-5	Comprehend A to D and D to A Converters.	15
CO-6	Comprehend PAL, PLA and FSM	15

Teaching and Examination Scheme:

Teaching / Learning Scheme (in Hours per semester)					Total Credits = TH/30	Assessment Pattern and Marks					Total Marks
L	T	P	PBL*	TH		Theory		Tutorial / Practical			
						ESE (E)	PA (M)	PA/ (I)	PBL (I)	ESE (V)	
60	00	30	30	120	04	70	30	20	30	50	200

Where L = Lecture, T= Tutorial, P= Practical, TW/SL = Term-Work / Self-Learning, TH = Total Hours, PA = Progressive Assessment, ESE = End-Semester Examination

* Problem Based Learning (PBL) aims to accommodate learning beyond syllabus as per clause 9.4 of NBA manual.

Content:



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Sr. No.	Content	Total Hrs
1	NUMBER SYSTEM: Digital computer and digital systems, Binary Number, Number base conversion Octal and Hexadecimal Number, complements, Binary Codes, Binary Storage and register, Binary Logic, Integrated Circuit	4
2	BOOLEAN ALGEBRA AND LOGIC GATES: Basic Definition, Axiomatic Definition of Boolean Algebra, Basic Theorem and Properties of Boolean Algebra, Min terms And Maxterms, Logic Operations, Digital Logic Gates, IC digital Logic Families	4
3	SIMPLIFICATION OF BOOLEAN FUNCIONS: Different types, K Map method, Product of sum Simplification, NAND or NOR implementation, Don't Care condition, Tabulation method	4
4	COMBINATIONAL LOGIC: Introduction, Design Procedure, adder, subtractor, Code Conversion, Universal Gate	4
5	COMBINATIONAL LOGIC WITH MSI AND LSI: Introduction, Binary Parallel Adder, Decimal Adder, The look ahead carry Adder, Excess-3 Adder, Binary Multipliers, Parity bit Generators/checkers, Magnitude Comparator, Encoder, Decoder, Multiplexer, De- multiplexer, Hazards and hazards free realization .	6
6	SEQUENTIAL LOGIC: Introduction, Flip-Flops, Triggering of Flip-Flops, Analysis of Clocked Sequential Circuits, State Reduction and Assignment, Flip-Flop Excitation Tables, Design Procedure, Design of Counters,	4
7	REGISTERS, COUNTERS AND THE MEMORY UNIT: Introduction, Registers, Shift Registers, Ripple Counters, Synchronous Counters, Timing Sequences, Memory Unit, RAM, ROM, EPROM, EEPROM, Flash Memory	4
8	REGISTERS TRANSFER LOGIC & MICRO OPERATION: Introduction, Inter-register Transfer, Arithmetic, logic and shift Micro- Operations, Conditional Control Statements, Fixed-Point Binary Data, overflow, Arithmetic Shifts, Decimal Data, Floating-Point Data, Instruction Codes, Design of Simple Computer.	4
9	LOGIC FAMILIES: Digital IC specification Terminology: Threshold voltage, Propagation Delay, Power dissipation, Fan-in, Fan-out, Voltage and current parameters, Noise margin, Operating Temperature, Speed power product. Transistor Transistor Logic: Two input TTL NAND gate, Totem pole output, Current sinking, Current sourcing, TTL loading and Fan-out. Open Collector gates: Wired AND operation, Tri state TTL, Buffer/Drivers.	5



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10	A to D Converter and D to A Converter: Introduction to following Digital to Analog Converters : Weighted Resistor D/A Converter, R-2R Ladder D/A Converter, Specifications for D/A Converters, An Example of D/A Converter IC: Digital Input Codes, Analog output, Calibration, Sample and Hold, Analog to Digital Converters: Quantization and Encoding, Parallel Comparator A/D Converter, Counting A/D Converter, Dual Slope A/D Converter, A/D Converter Using Voltage to frequency conversation, A/D Converter Using Voltage to time conversation, Specification of A/D Converters An Example of A/D Converter IC: Operation , Digital Output, Analog Input, Calibration	6
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Suggested Specification table with Marks (Theory):

R Level	U Level	A Level	N Level	E Level	C Level
7	14	14	14	14	7

Legends: R: Remembrance; U: Understanding; A: Application, N: Analyze and E: Evaluate C: Create and above Levels (Revised Bloom’s Taxonomy)

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Reference Books:

1. M Morris Mano, “Digital Logic and Computer Design”, Person, LPE, 4th ed., 2009A. Anandkumar, “Fundamentals of Digital circuits”, PHI, Second Edition.
2. Malvino & Leach, “Principle of Digital Electronics”, MC Graw- Hill, 2nded, 1975
3. R.P. Jain, “Modern Digital Electronics”, McGraw-Hill, 4th ed. 2010.
4. Boyce J. C., “Digital Logic: Operation and Analysis”, Prentice Hall, 2nded., 1982

List of Experiments:

1. Verification of logic gates using digital ICs and configuring NAND and NOR gates as universal logic gates.
2. Implementation of Boolean Logic Functions using logic gates and combinational circuits, measure digital logic gates specifications such as propagation delay, noise margin, Fan-in and Fan-out
3. Design and implementation of Binary Half adder, full adder, half subtractor, full subtractor,



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Parallel adder.

4. Design and implementation of code converters.
5. Design and implementation of Encoder and Decoder.
6. Design and implement of Magnitude comparator.
7. Design and implementation of multiplexer and de-multiplexer.
8. Design and Implement JK-flip-flop, RS-flip-flop, D – flip-flop and T-flip-flop using digital Ics.
9. Design and implement universal shift registers using digital IC.
10. Design and implement Asynchronous and synchronous Counters.
11. Implement A to D Converter using trainer Kit.
12. Implement D to A Converter using trainer Kit.

Major Equipment: Digital Storage Oscilloscope (DSO), CROs, Multi-meters, Function generator, Bread board trainer, Logic gate ICs

List of Open Source Software/learning website:

1. Web packages for HDL, GHDL, Free HDL
2. PS pieces and N.G. Spice
3. X circuit and Scilab
4. NPTEL website and IITs virtual laboratory

• **List of suggested activities for Problem Based Learning:**

Sl. No.	Name of the activity	No. of hours	Evaluation Criteria
1.	Industry/Research laboratory visit	Visit = 5hrs., Report preparation = 5hrs. Total = 10hrs.	Based on report submitted. Report should contain observations and calculations based on industry/ lab data.
2.	Technical Video based learning related to the subject	Duration of video = 5hrs. Report preparation = 5hrs. Total = 10hrs.	Report /presentation based on the video learning outcomes.
3.	Assignment writing. Numericals based assignment is preferable.	5 assignments of 4hrs. each. Total = 20hrs.	Based on the correctness of submitted assignment.
4.	Problem solving/Coding using C, C++, MATLAB, Python,	5 small coding-based assignment of 2hrs. each. Total = 10hrs.	Based on the coding solution submitted.



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	SCILAB,modeling and Analysis software or any other software		
5.	Self-learning online course	Minimum duration of the course should be 10hrs.	Examination based assessment at the end of course. Based on the certificate produced.
6.	Identification and solution of Complex problem	Maximum 2 problems. Study of the problem and solution finding, Total = 10hrs.	Based on the depth of the solution submitted.
7	Videos on Industrial safety/Disaster Management aspects based on subject	Duration of video = 5hrs. Report preparation = 5hrs. Total = 10hrs.	Based on quiz/report submitted
8	Technical paper reading and summarization of research papers based on relevant subject	5 research papers = 20 hrs.	Summarize research paper and evaluation critical parameters
9.	Poster/chart/power point preparation on technical topics	Duration = 6 hrs.	Based on poster/chart preparation and presentation skills
10	Working/non-working model on technical topics	Working = 12 hrs. Non- working = 8 hrs.	Based on inter department/external evaluation
11	Industrial exposure for 2-3 days to observe and provide tentative solutions on society/environment/health/sustainability/any other issue	Duration = 15 hrs. for industrial exposure Problem identification and tentative solution = 10 hrs. Total = 20 hrs.	Based on evaluation of critical problems and solutions
12	Group Discussion on emerging/trending technical topics based on subject	Duration = Min. 1 hr.per subject. Max. 3 hrs. per subject	Based on performance in group discussion, technical depth, knowledge etc.
13.	Real world case studies-based learning	Duration of data collection/study = 5hrs. Report preparation = 5hrs.	Based on in-depth study, technical depth, data collected, fact finding, etc.



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		Total = 10hrs.	
14.	Application/Software development	Duration = 10 hrs.	Depending on the complexity of the Application/Software
15.	Research paper publication	Duration = 10 hrs.	Based on submission of proof of publication
16.	Upgradation/Reverse engineering studies of existing equipment of the laboratory	Duration 10 hrs.	Based on the performance of the equipment
17.	Expert lecture/session	Duration 3 hrs. For attending the lecture/session– 2 hrs. and for report writing 1 hr.	Based on the proof of attendance and report submitted
18.	Annotated Video Explanation of Concept/Problem	10h (Preparation + Recording + Submission)	Based on accuracy of explanation, clarity, and presentation style.
19.	Patent Search and Innovation Gap Identification	10h (Search + Report)	Based on number of relevant patents analyzed and identification of innovation scope.

Note:

1. All the suggested activity should be related to the subject.
2. The number of hours are suggestive. Faculty can sub-divide the number of hours based on the activity. However, total number of hours is fixed.
3. Rubrics for the evaluation can be prepared by the faculty.
4. Subject teacher can add the relevant activities other than those listed above, with the consent of head of the department and DQAC.
