GUJARAT TECHNOLOGICAL UNIVERSITY

Program Name: Bachelor of Engineering
Level: UG
Subject Code: BE03000021
Subject Name : Digital Electronics

WEF Academic Year:	2024 - 2025
Semester:	3
Category of the Course:	Professional Core Course

Prerequisite :	Not Applicable
Rationale :	Various number system, basic digital elements, combinational and sequential circuits and various logic families

Course Outcome:

After Completion of the Course, Student will able to:

No	Course Outcomes	RBT Level*
01	Understand different number system	RM/UN
02	Understand Boolean Algebra, Logic gates and its simplification	UN
03	Demonstrate combinational and sequential circuits	AP
04	Analyze combinational and sequential logic circuits	AN
05	Validate different logic family terminologies	EL

*RM: Remember, UN: Understand, AP: Apply, AN: Analyze, EL: Evaluate, CR: Create

Teaching and Examination Scheme :

Teaching - Learning Scheme (in Hours per Semester)					Total Credits = TH/30	Assessment Pattern and Marks					Total Marks
						Theory		Tutorial / Practical			
L	T	P	PBL*	TH		ESE (E)	PA (M)	PA/ (I)	PBL (I)	ESE (V)	
45	0	30	45	120	04	70	30	20	30	50	200

Course Content:

Sr. No.	Course Content	No. of Hours	% of Weightage
1	**BINARY SYSTEM:** Digital computer and digital systems, Binary Number, Number base conversions, Octal and Hexadecimal Number, Complements, Binary Codes, Binary Storage and register, Binary Logic, Integrated Circuit	3	6

2	**BOOLEAN ALGEBRA AND LOGIC GATES:** Basic Definitions, Axiomatic Definition of Boolean Algebra, Basic Theorems and Properties of Boolean Algebra, Boolean Functions, Canonical and Standard Forms, Minterms And Maxterms, Logic Operations, Digital Logic Gates	6	14
3	**SIMPLIFICATION OF BOOLEAN FUNCIONS:** The Map Method, 2, 3, 4, 5 and 6 variable maps, Product of sums simplification, NAND, NOR & other two level implementations, Don't Care Conditions, Tabulation Method and Determination and Selection of Prime-Implicants	6	14
4	**COMBINATIONAL LOGIC:** Introduction, Design Procedure, Adder, Subtractor, Code Conversion, Universal Gate and multilevel NAND and NOR circuits, Exclusive OR and Equivalence functions.	5	11
5	**COMBINATIONAL LOGIC WITH MSI AND LSI:** Introduction, Binary Parallel Adder, Decimal Adder, The look ahead carry Adder, Excess-3 Adder, Binary Multipliers, Parity bit Generators/checkers, Magnitude Comparator, Encoder, Decoder, Multiplexer, De-multiplexer.	5	11
6	**SEQUENTIAL LOGIC:** Introduction, Flip-Flops, Triggering of Flip-Flops, Analysis of Clocked Sequential Circuits, State Reduction and Assignment, Flip-Flop Excitation Tables, Design Procedure, Design of Counters, Design with State Equations, The finite state model, Synthesis of synchronous sequential circuits, Serial Binary adder with Moore type FSM, The sequence Detector - Mealy type model and Moore type circuit.	5	11
7	**REGISTERS, COUNTERS AND THE MEMORY UNIT:** Introduction, Registers, Shift Registers, Ripple Counters, Synchronous Counters, Timing Sequences, Memory Unit – Role of memory in a computer system, memory types and terminology, Semiconductor RAM's, Non volatile RAM's, Magnetic Memories, Optical Disk Memory and Charged Coupled Devices.	5	11
8	**REGISTERS TRANSFER LOGIC & MICRO OPERATION:** Introduction, Inter-register Transfer, Arithmetic, logic and shift Micro-Operations, Conditional Control Statements, Fixed-Point Binary Data, overflow, Arithmetic Shifts, Decimal Data, Non – numeric Data, Floating-Point Data, Instruction Codes, Design of Simple Computer.	5	11

9	**DIGITAL INTEGRATED CIRCUITS:** Characteristics: Threshold voltage, Propagation Delay, Power dissipation, Fan-in, Fan-out, Voltage and current parameters, Noise margin, Operating Temperature, Speed power product. Transistor Transistor Logic: Two input TTL NAND gate, Totem pole output, Current sinking, Current sourcing, TTL loading and Fan-out. Open Collector gates: Wired AND operation, Tri state TTL, Buffer/Drivers.	5	11
	Total	**45**	**100**

Reference Book:

1. M. Morris Mano, "Digital Logic and Computer Design", Person India, LPE, 2017
2. A. Anand Kumar, "Fundamentals of Digital circuits", PHI, 4th Edition, 2016
1. Rahul Dubey, "An Introduction to Internet of Things: Connecting Devices, Edge Gateway, and Cloud with Applications", Cengage India Publication
2. Raj Kamal, "Internet of Things: Architecture and Design Principles, Mc Graw Hill Education
3. Hanes et al "IoT Fundamentals", Cisco Press
4. Vijay Madisetti and ArshdeepBahga, "Internet of Things (A Hands-on-Approach)", , Paperback, 2015.
5. A. McEwen, H. Cassimally, "Designing the Internet of Things", Wiley, 2013.
6. YashwantKanetkar, "21 Internet of Things Experiments", Kindle edition
7. AdeelJaved, "Building Arduino projects for Internet of Things", Apress publication
8. Donald Noris, "The Internet of Things: Do it yourself Projects with Arduino, Raspberry PI and
9. BeagleBone Black" Mc Graw Hill Publication
10. Adrian McEwen & Hakim Cassimally, "Designing the Internet of things", Willey publication
11. Rahul Dubey, "An Introduction to Internet of Things: Connecting Devices, Edge Gateway, and Cloud with Applications", Cengage India Publication
12. Raj Kamal, "Internet of Things: Architecture and Design Principles, Mc Graw Hill Education
13. Hanes et al "IoT Fundamentals", Cisco Press
14. Vijay Madisetti and ArshdeepBahga, "Internet of Things (A Hands-on-Approach)", , Paperback, 2015.
15. A. McEwen, H. Cassimally, "Designing the Internet of Things", Wiley, 2013.
16. YashwantKanetkar, "21 Internet of Things Experiments", Kindle edition
17. AdeelJaved, "Building Arduino projects for Internet of Things", Apress publication
18. Donald Noris, "The Internet of Things: Do it yourself Projects with Arduino, Raspberry PI and
19. BeagleBone Black" Mc Graw Hill Publication
20. Adrian McEwen & Hakim Cassimally, "Designing the Internet of things", Willey publication
21. Rahul Dubey, "An Introduction to Internet of Things: Connecting Devices, Edge Gateway, and Cloud with Applications", Cengage India Publication

Suggested Course Practical List:

1. To verify and interpret the logic and truth table for AND, OR, NOT, NAND, NOR, Ex-OR, Ex-NOR gates.
2. To Realization of logic functions with the help of universal gates NAND and NOR Gate
3. To Verify De-Morgan's laws
4. To analyze the truth table of binary to gray and gray to binary converter
5. To design and verify operation of Half adder and Full adder.
6. To design and verify operation of Half Subtractor and Full Subtractor.
7. To design and verify operation of 4-bit full adder using IC 7483.
8. To design and verify operation of Encoder.
9. To design and verify operation of Decoder.
10. To design and implementation of 2-Bit Magnitude Comparator using logic gates and 4-Bit Magnitude Comparator using IC 7485.
11. Implementation of 4 X 1 Multiplexer using Logic gates and study of IC74151.
12. Implementation of 1X 4 Demultiplexer using Logic gates and study of IC 74154.
13. To verify the truth table of RS, JK, T and D flip-flops by using NAND & NOR gates ICs.
14. To analyze the circuit and truth table of 4-bit Bidirectional Universal shift register by using IC 74194.
15. To design and implement Asynchronous and synchronous Counters.
16. To design and verify the BCD counter using IC7490.
17. To simulate Logic circuits using Multisim simulator

List of Laboratory/Learning Resources Required:

1. Common Lab Manual (DTE)
2. Virtual Laboratory (vLab.co.in)
3. NPTEL Website

- **List of suggested activities for Problem Based Learning:**

Sr. No.	Name of the activity	No. of hours per activity	Evaluation Criteria
1.	Industry/Research laboratory visit	Visit = 5h, Report preparation = 5h Total = 10h	Based on report submitted. Report should contain observations and calculations based on industry/ lab data.
2.	Technical Video based learning related to the subject	Duration of video = 5h Report preparation = 5h Total = 10h	Report /presentation based on the video learning outcomes.
3.	Assignment writing. Numerical based assignment is preferable.	5 assignments of 2h each. Total = 10h	Based on the assignment submitted.
4.	Problem solving/Coding using C, C++, Python, SCILAB,	5 small coding-based assignment of 2h each.	Based on the coding solution submitted.

	MATLAB, MS-EXCEL or any other relevant software	Total = 10h	
5.	Self-learning on-line course	Minimum duration of the course should be 10h.	Examination based assessment at the end of course. Based on the certificate produced.
6.	Complex problem solving	Maximum 2 problem. Study of the problem and solution finding, Total = 10h	Based on the depth of the solution submitted.
7	Videos on Industrial safety aspects based on subject	Duration of video = 5h Report preparation = 5h Total = 10h	Based on quiz/report submitted
8	Discussion on research paper based on relevant subject	5 research paper = 20 h	Summarize research paper and evaluation critical parameters
9.	Poster/chart/power point preparation on technical topics	Duration = 6 h	Based on poster/chart preparation and presentation skills
10	Working/non-working model on technical topics	Working = 12 h Non- working = 8 h	Based on inter department/external evaluation
11	Industrial exposure for 2-3 days to observe and provide tentative solutions on society/environment/health/any other issue	Duration = 15 h for industrial exposure Problem identification and tentative solution = 10 h Total = 20 h	Based on evaluation of critical problems and solutions
12	Group Discussion on emerging/trending technical topics based on subject	Duration = 1 h each	Based on performance in group discussion, technical depth, knowledge etc.
13.	Real world case studies-based learning	Duration of data collection/study = 5h Report preparation = 5h Total = 10h	Based on in-depth study, technical depth, data collected, fact finding, etc.
14.	Application/Software development	Duration = 10 h	Depending on the complexity of the Application/Software
15	Online Technical Quizzes/Simulations	Multiple quizzes summing up to 10h	Based on quiz scores and reflection report after each quiz.
16	Patent Search and Innovation Gap Identification	10h (Search + Report)	Based on number of relevant patents analyzed and identification of innovation scope.

Note:

- All the suggested activity should be related to the subject.
- Subject coordinator shall identify activities from above list as per the subject needs, they also declare list of activities wise hours, evaluation scheme and rubrics to students at the start of semester.
- The number of hours is suggestive. Faculty can sub-divide the number of hours based on the activity. However, total number of hours is fixed.
- All records pertaining to the evaluation and assessment of self-learning activities must be properly maintained and preserved at the institute level. These records should be made available to the university upon request.
- Institutes are encouraged to utilize digital platforms, such as Microsoft Teams, for effective record-keeping and to ensure transparency in the evaluation and assessment of self-learning activities.

* * * * * * *