

# **GUJARAT TECHNOLOGICAL UNIVERSITY**

**M.E. Semester: III**

## **Signal Processing & VLSI Technology (EC)**

**Subject Name: VLSI Design Laboratory**

**Subject Code: 732601**

Each student will have to carry out about 10-12 practicals involving analysis, design and testing of substantial hardware modules using any front end tools with implementation on FPGA/CPLD and also some layout exercises using backend tools. It is compulsory for each student to carry out a **VHDL/Verilog based mini project**