GUJARAT TECHNOLOGICAL UNIVERSITY

M.E. Embedded Systems (Branch Code - 54)

Year – I (Semester – II) (W.E.F. January 2014)

Subject Name: Embedded and VSLI Signal Processing -Major Elective II (725404)

Course Content:

Sr. No.	Course Contents	Hours
1	**Digital Signal Processing Overview:** Signals, Systems and Signal processing, classification of signals, Linear Time Invariant (LTI) System, Convolution, And Correlation: Properties and application of correlation, Sampling, Z-transform, FFT Algorithms and Fundamentals of FIR and IIR Filters.	**20**
2	Introduction to hardware description language (VHDL): Structural, Behavioral and Data Flow modeling, Concurrent and Sequential VHDL, VLSI Design methodologies, FPGA Technology and its Applications, The FPGA technology roadmap, FPGA Architecture and its building blocks, Technology mapping for FPGAs.	**10**
3	Design and Implementation using CPLD and FPGA and need of Floor Planning and placement tools, FPGA memory and registers, Input/output blocks and requirements and Configurable Logic Blocks, FPGA Families and Sources, xiling 3000 series logic cell with its CLB.	**08**
4	FPGA elements for DSP algorithms, Building delay lines and Shift Registers, Use of RAM and ROM (memory) on FPGAs, Multiplexers for channel selection.	**08**
5	DSP Arithmetic Essentials, Fundamental adders and multiplier arrays, Signal Flow Graph (SFG) Techniques, FPGA design for digital filters: FIR and IIR Filter.	**08**
	Total	**54**

Reference Book:

1. John G. Proakis, "Digital Signal Processing" Principles, Algorithms and applications, Prentice-Hall of India, 2007, fourth edition.
2. K. K. Parhi, "VLSI Digital Signal Processing Systems- Design and Implementation", John Wiley & Sons, Inc., 1999, fourth edition.
3. Sanjit K. Mitra, "Digital Signal Processing: A Computer based approach", McCraw Hill, 1998, second edition
4. J. Bhasker, VHDL Synthesis Primer, Pearson Education Asia, Low Price, Edition, second edition

5. Uwe MeyerBaese: “Digital Signal Processing with Field Programmable Gate Arrays”, Springer, 2001, second edition.
6. Xilinx and Altera Application notes on the architecture of FPGA and CPLD