GUJARAT TECHNOLOGICAL UNIVERSITY
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M.E (VLSI & EMBEDDED SYSTEMS DESIGN)

SEMESTER II

STRUCTURE AND SYLLABUS (w.ef. January 2012)

Subject code	Subject Name	Teaching Scheme (Hour)			Credit
725201	Digital VLSI Design II- Backend	4	0	0	4
725202	Embedded System Hardware Design	4	0	0	4
725203	Analog and Mixed Signal IC Design	4	0	0	4
725204	Protocols and Interfaces (Elective II)	4	0	0	4
735205	Design For Testability (Elective II)	4	0	0	4
735206	Standard Cell Library and Memory Design (Elective II)	4	0	0	4
725207	LAB 4	0	0	8	3
725208	LAB 5	0	0	8	3
725209	LAB 6	0	0	8	3

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SEMESTER II (w.ef. January 2012)

Subject Code: 725201
Subject Name: Digital VLSI Design II - Backend

Sr_No	Particular
1.	**Objective:** The study of IC design basics, levels, strategies, options, implementation methods, styles, challenges, and trends especially back-end. In the process of the laboratory work it is necessary to study the main IC design tools and to implement the basic digital electronic circuits' design flow.
2.	**Lecture:** **UNIT I – Recap of Front-end flow and Logic Synthesis.** Recap Units II and IV of Course Digital VLSI Design I – Front-end.
3.	**UNIT II – Physical Design Setup and Floorplanning** VLSI Design Cycle, Methodology of Physical Design, Simplified Cycle of Physical IC Design, Partitioning, Floorplanning, Placement, Routing, Compaction, Verification. Logical libraries, Physical Libraries, Timing Constraints, Database format, Logical data setup, Physical data setup, Technology Files, Interconnect delay models, tcl scripting for automation. Hierarchical Design Planning Flow, Pad Creation and Order Assignments, Core Area, Initializing the Floorplan, Timing Driven Placement, Placement with Hierarchical Gravity, Analyze placement and Color Modules, Post-initialization Macro placement controls, Large Macro Handling, Power Network Synthesis (PNS), Power Network Analysis (PNA).
4.	**UNIT III – Placement** Placement Methodology, Fast Iteration with Coarse Placement, Understanding the Congestion Calculation, Textual Congestion Report, Analyzing the Congestion Map, Global Route (GR) for Congestion Map, Strategies for Fixing Congestion Problems, Congestion-Driven Placement Options, Adjusting Cell Density, Timing and Power Optimization for Best QoR, Congestion-Driven Placement, Incremental Congestion Refinement, Refinement Flow, Incremental mode, Area Recovery, Timing Analysis.
5.	**UNIT IV – Clock Tree Synthesis** Design Status, Start of CTS Phase, Clock Tree Synthesis, CTS Goals, Define Clock Root Attributes, Stop, Float and Exclude Pins, Generated and Gated Clocks , User-defined or Explicit Stop Pins, Defining an Explicit Float Pin, Preserving Pre-Existing Clock Trees, Impact of Preexisting Clock Cells, Logical Design Rule Constraints, Non-Default Clock Routing, Specifying Non-Default

	Rules, Nondefault Rule Options, Effects of Clock Tree Synthesis, Incremental Placement / Optimization, Analysis using the CTS GUI , Clock Tree Optimization, Inter-Clock Delay Balancing, Post Route CTO.
6.	**UNIT V – Routing and Post Tapeout flow** Design Status, Start of Routing Phase, Grid-Based Routing System, Routing over Macros, Pre-Route Checks, Routing Operations, Core Routing Strategy, Fixing DRC Violations, Crosstalk-Induced Noise, Crosstalk-Induced Delay, Crosstalk Prevention, Crosstalk Correction, Wire Sizing.
7.	**Labs :** Tools used during laboratory works: Design Compiler and IC Compiler.
8.	**Course Project:** A project of suitable complexity, comprising of RTL coding, Synthesis and complete netlist to GDSII flow must be completed.
9.	**Course Material:** The field of VLSI and Embedded Systems is getting updated constantly and to keep up to date with the latest research, technology and industry trends, Instructor for this course will decide and provide the course material. This could be a combination of slides or research material or text book references or any other relevant documentation depending on a) the nature of the curriculum and b) relevant skills to be imparted as outcome of the course.

References:

- J.P. Uyenmura. Introduction to VLSI Circuits and Systems, J.Wiley & Sons, 2002.
- J.M. Rabaey, A. Chandrakasan, B. Nikolic. Digital Integrated Circuits - A Design Perspective, Prentice Hall, 2003.
- J.P. Uyenmura. Modern VLSI Design - System-on-Chip Design, Prentice-Hall, 2002.

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SEMESTER II

Subject Code: 725202
Subject Name: Embedded Systems Hardware Design

SR_NO	PARTICULAR
1.	**Objective:** The main objective of this course is to study and understand the concepts of embedded systems and its hardware. In the process of the laboratory work it is necessary, using schematic simulator tool to simulate and check the circuits designed with respect to the laboratory task assignment, to draw and analyze steady-state characteristics and transient processes, analyze the impact of process and environment parameter variations on the circuit performance.
2.	**Lecture:** **UNIT I: Introduction to Embedded Systems** Definition and Classification – Overview of Processors and hardware units in an embedded system – Software embedded into the system – Complex System Design Embedded Systems on a Chip (SoC) and the use of VLSI designed circuits
3.	**UNIT II: Microcontrollers and Processor Architecture** 8051 architecture, Input / Output ports and circuits, External memory, Counter and Timers, PIC Controllers, Interfacing Processor (8051, PIC), Memory Interfacing, I/O devices, Memory Controller and Memory Arbitration schemes
4.	**UNIT III: Introduction to PCB Fabrication** The importance of interconnects. The basics. History and evolution. Component selection. Bill of materials. Specification and classification of PCBs. Techniques of layout design. Artwork generation methods - manual and CAD. General design factor for digital and analog circuits. Layout and artwork making for SS, DS and ML Boards. Design for manufacturability. A review of specification design standards. Introduction to PCB technology. Anatomy of laminates, resins, reinforcing materials.

	Phototool generation including screen preparation. Imaging techniques. PCB Fabrication techniques-single, double sided and multilayers. Drilling operation-manual and CNC. Etching: chemical principles and mechanisms. Plating operations manual and automated. Post operations-stripping, black oxide coating and solder masking. PCB component assembly processes. Environmental concerns in PCB industry.
5.	**UNIT IV: PCB Layout** Embedded Hardware & Firmware Design and Development Analog &Digital Electronic components, VLSI & Integrated circuit design, Electronic Design Automation tools , PCB layout Design and its fabrication .Embedded firmware design approaches , Board design theory and application, multi-layer PCB boards, signal integrity and noise handling, auto-routing, manufacturing.
6.	**UNIT V: Hardware/Software Co-design** Co-design Methodologies; Code Generation for Rapid Prototyping; Power Consumption Issues; Applications
7.	**Lab** Tools used during laboratory works: Encore or any other related tool. • Study of creating package symbols (schematic and layout). • Study of LVDS, SSTL PCB Layout guidelines. • Selective system design
8.	**Course Project:** A project of suitable complexity, comprising of program design, coding, compilation and debug must be completed.
9.	**Course Material:** The field of VLSI and Embedded Systems is getting updated constantly and to keep up to date with the latest research, technology and industry trends, Instructor for this course will decide and provide the course material. This could be a combination of slides or research material or text book references or any other relevant documentation depending on a) the nature of the curriculum and b) relevant skills to be imparted as outcome of the course.

References:

- Rajkamal, Embedded Systems Architecture, Programming and Design, TATA McGraw-Hill, First reprint Oct. 2003
- Steve Heath, Embedded Systems Design, Second Edition-2003, Newnes, David E.Simon, An Embedded Software Primer, Pearson Education Asia, First Indian Reprint 2000.
- Wayne Wolf, Computers as Components; Principles of Embedded Computing System Design - Harcourt India, Morgan Kaufman Publishers, First Indian Reprint 2001
- Frank Vahid and Tony Givargis, Embedded Systems Design - A unified Hardware /Software Introduction, John Wiley, 2002.

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SEMESTER II

Subject Code: 725203
Subject Name: Analog and Mixed Signal IC Design

SR_NO	PARTICULAR
1.	**Objective :** The main objective of the course is to study analog integrated circuits features, design and analysis methods of analog and mixed signal circuits.
2.	**Lecture:** **UNIT I – Review of transistor operation, Single stage amplifiers, Differential amplifier** MOS I/V characteristics. Transistor second order effects. Small signal analysis. Small signal model.Gain of common-source stage amplifier using small signal analysis. Common-source stage with resistive load, diode-connected load, current-source load, triode load, source degeneration. Source follower stage. Common-gate stage. Cascode stages.Single-ended and differential operation. Basic differential pair.Common-mode response. Differential pair with MOS loads. Gilbert Cell.
3.	**UNIT II - Current Mirrors, Response of Amplifiers, Noise characteristics** Basic and cascode current mirrors. Using active current mirrors as loads. The Miller theorem. Frequency response of source follower, common-gate amplifier, cascode stage, differential pair.Noise characteristics. Noise types: thermal noise, flicker noise. Representation of noise in circuits. Properties of feedback circuits. Feedback Configurations. Effect of loading in feedback.
4.	**UNIT III - Operational amplifiers** Operational amplifier's performance parameters. One-Stage Op Amps. Two-Stage Op Amp. Op Amps Gain Boosting. Op Amps Common-Mode Feedback. Op Amps Input Range Limitation: unity-gain buffer, extension of input CM range, variation of equivalent transconductance with the input CM level. Op Amps Slew Rate. Noise in Op Amps and Power Supply

	Rejection.Stability and Frequency compensation.
5.	**UNIT IV - Bandgap References, Switched-capacitor circuits, Nonlinearity** Supply-independent biasing. Temperature- independent references: negative-TC voltage, positive-TC voltage, bandgap reference. PTAT current generation. Speed and noise issues. Continuous-time feedback amplifier using resistors, capacitors, switched-capacitor amplifier in sampling mode, amplification mode, transfer of capacitor's charges. Sampling switches. Switched-capacitor amplifiers. Switched-capacitor integrator. Nonlinearity. Mismatch. Ring oscillators. LC oscillators. Voltage-controlled oscillators. Mathematical models of VCOs.
6.	**UNIT V- Phase-locked loops, Data converters, charge-coupled devices (CCD)** Simple PLL.Charge-pump PLLs.Non ideal effects in PLLs: PFD/CP non idealities, jitter in PLLs.Delay-locked loops.PLL applications. Analog versus discrete time signals. Sample and hold characteristics.ADC and DAC specifications.DAC architectures.ADC architectures. Sampling and aliasing, Quantization noise & Data converter SNR. CCD imaging and architecture.
7.	**Labs:** Tools used during laboratory exercises are Custom Designer, WaveView and HSpice.
8.	**Course Project:** A project of suitable complexity including Analog design of a circuit, simulation and analysis must be completed.
9.	**Course Material:** The field of VLSI and Embedded Systems is getting updated constantly and to keep up to date with the latest research, technology and industry trends, Instructor for this course will decide and provide the course material. This could be a combination of slides or research material or text book references or any other relevant documentation depending on a) the nature of the curriculum and b) relevant skills to be imparted as outcome of the course.

.**References:**

1. R.J. Baker, H.W. Li, D.E. Boyce. CMOS. Circuit design, Layout, and Simulation (2nd Edition), 2005. 1038p.
2. P. Horowitz, W. Hill, Electronic Circuit Design: Art and Practice, 2001. 192p.
3. B. Razavi, Design of Analog CMOS Integrated Circuits, 2000. 684p.
4. R.J. Baker, CMOS Mixed-Signal Circuit Design, 2002. 502p
5. B. Razavi. Principles of Data Conversion System Design. 1994. 272P

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SEMESTER II

Subject Code: 725204
Subject Name: Protocols and Interfaces

SR_NO	PARTICULAR
1.	**Objective:** The study of architectural elements, performance metrics and system architecture of computer systems with a focus on interfaces and protocols. In the process of the laboratory work it is necessary to use and study standard and emerging architectures.
2.	**Lecture:** **UNIT I - Introduction (Recap)** Basic concepts of computer organization. The stored program model. Classes of computer architecture. Processor vs. System architecture. Elements of computer systems – processors, memories, I/Os, disks, buses etc.
3.	**UNIT II - Data Processing in Microcontrollers** Programs based on data transfer, arithmetical, logical, branching, bit (Boolean) operation instructions.
4.	**UNIT III - Organization communications of Microcontroller with the object of control** Data Transfers between On-chip hardware Microcontroller and peripheral Units. Signal processing and conditioning. Timing Function conditioning. Software conversion of codes. Software support of A/D and D/A Converters.
5.	**UNIT IV - Interfacing with Microprocessor Systems** Organization communications of Operator with Microcontroller. Keyboard and Display interfacing. Input/ output enhancement mode
6.	**UNIT V- Protocols** Types of memory interfaces – SRAM, DRAM, Flash, EPROM/ROM and corresponding protocols. Types of Disk protocols – SATA, IDE, SCSI Special memories – Video RAMs, RDRAM, CAM Interrupt controllers, priorities and arbitration. ISRs and context

	saving architectures. Programmable interrupt controller PCI, USB, 1394, Ethernet, 802.11x, PCI Express, ACPI Bridge functions Storage area networks and protocols
7.	**Labs :** Tools used during laboratory works: Linux, Perl, Gcc,Gdb, VCS • Study and implementation of interfacing exercises. • Study and implementation of performance of memory systems and their impact on system performance • Study and implementation of Standard interfaces
8.	**Course Project:** A project of suitable complexity, comprising of program design, coding, compilation and debug must be completed.
9.	**Course Material:** The field of VLSI and Embedded Systems is getting updated constantly and to keep up to date with the latest research, technology and industry trends, Instructor for this course will decide and provide the course material. This could be a combination of slides or research material or text book references or any other relevant documentation depending on a) the nature of the curriculum and b) relevant skills to be imparted as outcome of the course.

References:

- Computer Architecture, A Quantitative approach by D.Patterson and J. Hennessy
- Computer Organization by D. Patterson and J.Hennessy
- Bus Specifications - PCI, PCIe, SCSI, IDE, USB, 802.11x, SATA

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SEMESTER II

Subject Code: 735205
Subject Name: Design for Testability

Sr_No	PARTICULAR
1.	**Objective:** The main objectives of the course are to study the basics of VLSI design with embedded test circuits and to study the principles of design, analysis and simulation of self-testable digital IC.
2.	**Lecture:** **UNIT I – Introduction** The need for testing, Fabrication, Assembly and Test Process Flows.
3.	**UNIT II – Scan Testing** Using additional primary inputs and outputs to improve controllability and observability, Scan-based testing. Design rules, Ways to overcome rule violations. Automated Test Pattern Generation for scan testing. Scan test protocol, Full-scan and partial scan, Automated scan design systems, Scan design flow, Scan design overhead: area, timing, power considerations.
4.	**UNIT III - Built-in self testing (BIST)** BIST architecture, Test compression methods, Random and weighted random pattern testability, BIST Pattern generator and response analyzer, Theory of Linear feedback shift registers (LFSR), Generating test vectors and Signature analysis, Scan-based BIST architecture, Built-in Logic Block Observation (BILBO), Test point insertion for improving random testability, Memory IC BIST and Built-In self repair.
5.	**UNIT IV - Boundary Scan Testing** Boundary scan technique. JTAG standard (IEEE 1149.1), Application of Boundary scan for PCB testing, Boundary scan instructions, Boundary Scan Description Language (BCDL), Boundary scan Test access port (TAP), TAP controller, Boundary scan instructions, Instruction register, Test data register. Boundary scan register, TAP controller state diagram, Testable design flow, Using Boundary scan TAP for IC internal circuit testing.

6.	**UNIT V : Boundary Scan Testing II** Boundary scan instructions, Instruction Register, Test Data register. Boundary scan register, TAP, controller state diagram, Testable design flow, Using Boundary scan TAP for IC internal circuit testing
7.	**Labs:** The labs will include: Introduction to Design Vision Study of scan testing in DFT Compiler environment Test pattern generation in TetraMax ATPG Tools used during laboratory exercises are VCS, Design Vision, TetraMax and DFT Compiler.
8.	**Course Project:** A project of suitable complexity, comprising of program design, coding, compilation and debug must be completed.
9.	**Course Material:** The field of VLSI and Embedded Systems is getting updated constantly and to keep up to date with the latest research, technology and industry trends, Instructor for this course will decide and provide the course material. This could be a combination of slides or research material or text book references or any other relevant documentation depending on a) the nature of the curriculum and b) relevant skills to be imparted as outcome of the course.

References:

B. Friedman. Digital Systems Testing and Testable Design. Jaico Publishing House. 2005. 670p.

M. L. Bushnell and V. D. Agrawal. Essentials of Electronic Testing, Kluwer Academic Publishers, 2000, 709p.

M. Abramovici, M.A. Breuer, A.D. Friedman. Digital Systems Testing and Testable Designs. 1998.

Neil H.E. Waste, K. Eshraghian. Principles of CMOS VLSI Design. Addison Wesley; 2 edition, 1994. 735p.

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SEMESTER II

Subject Code:735206
Subject Name: Standard Cell Library and Memory Design

Sr_No	Particular
1.	**Objective:** The study of IC standard cell elements, memory types, memory failures, memory and cell characterization and testing. In the process of the laboratory work it is necessary to study the main IC design tools and to implement electronic circuits in the form of standard cells and memories.
2.	**Lecture:** **UNIT I– Introduction** IC design flows. Use of standard cell elements vs. custom design and Gate array paradigms. Introduction to memory types and construction of memory elements.
3.	**UNIT II - Standard cell library composition and usage** Types of standard cell elements. Logical and functional elements, primitives and complex macros. Sequential elements and register files. (Flip flop and latch design). Data path elements. Library size vs. usage in standard flows. Drive strength and cell families. Layout of library elements – single height, double height cells. Power Management cells.
4.	**UNIT III - Standard cell characterization** Usage of standard cells by various tools. Information needed at each stage of design flow. Characterization parameters, setup and runs across PVT corners. Library representation formats. (Gate level simulation, synthesis, timing, layout, timing, LVS, DRC)
5.	**UNIT IV - Memory elements and array design.** Volatile and Non-volatile RAM, ROM,EPROM, Flash (EEPROM), OTP elements and cell design. State retention volatile memories. Array design – architecture, bitline/wordline optimization, sense-amps and mux/demux architecture. Memory banking, refresh cycle management. Multi-port memories. Cache memories. Special memories such as CAMs.

6.	**UNIT V– Memory defects, failures and testing, layout and characterization** Memory defects and repair. Temporal failures, Soft errors. Membist and other test techniques for memories. Memory layout and its impact on performance. Characterization of memories – timing, area, power parameters. Layout views – hard macro representation, keep outs and congestion impact.
7.	**Lab :** Tools used during laboratory works: EDA tools using Synopsys EDK 90nm library. Study and implementation of standard cell library element Study and implementation of small register file from standard cell Study and implementation of memory element (SRAM 6 T cell) Study and implementation of memory array (SRAM)
8.	**Course Project:** A project of suitable complexity, comprising of program design, coding, compilation and debug must be completed.
9.	**Course Material:** The field of VLSI and Embedded Systems is getting updated constantly and to keep up to date with the latest research, technology and industry trends, Instructor for this course will decide and provide the course material. This could be a combination of slides or research material or text book references or any other relevant documentation depending on a) the nature of the curriculum and b) relevant skills to be imparted as outcome of the course.

References:

Standard cell and memory library documentation by Vendors
90nm EDK library