

# GUJARAT TECHNOLOGICAL UNIVERSITY

## M.E.in VLSI System Design

### Semester: I

Subject Name: **Principles of VLSI Design**

Subject Code: **714201**

Sr. No	Course Content	Total Hrs
1.	<b>Introduction:</b> VLSI Design Flow, Design Styles ASIC Design flow, Design Methodologies, Introduction to MOSFETs: Basic principle of MOS Transistor.	5
2.	<b>Fabrication of MOS Transistor</b>	10
3.	<b>The MOS Inverter: Static and Switching Characteristics</b> Inverter principle, Depletion and enhancement load inverters, the basic CMOS inverter, and transfer characteristics, logic threshold, Noise margins, and Dynamic behavior, Propagation Delay, Power Consumption.	14
4.	<b>MOS Circuit Layout &amp; Simulation:</b> MOS SPICE model, device characterization, Circuit characterization, interconnects simulation. MOS device layout: MOS Layers Stick/Layout Diagrams, Transistor layout, Inverter layout.	7
5.	<b>Combinational MOS Logic Design: Static MOS design:</b> Complementary MOS, Rationed logic, Pass Transistor logic, complex logic circuits.	8
6.	<b>Dynamic MOS design:</b> Dynamic logic families and performances.	5
7.	<b>Sequential MOS Logic Design</b> Static latches, Flip flop & Registers, Dynamic Latches & Registers, CMOS Schmitt trigger, Monostable sequential Circuits, Astable Circuits. Memory Design: ROM & RAM cells design	9
8	<b>BiCMOS Logic Circuits</b> Overview and Applications of BiCMOS Circuits	5

**Laboratory Work:** It will consist of 10 to 12 experiment based on above syllabus.

#### Reference Books:

1. S.M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, Third Edition, MHI.
2. W. Wolf, Modern VLSI Design: System on Chip, Third Edition, PH/Pearson
3. N. Weste, K. Eshraghian and M. J. S. Smith, Principles of CMOS VLSI Design: A system Perspective, Second Edition (Expanded) AW/ Pearson.
4. J. M. Rabaey, A. P. Chanrakasan and B. Nikoli, Digital Integrated Circuits: A Design Perspective, Second Edition, PH/Pearson.
5. D.A Pucknell and K. Eshraghian, Basic VLSI Design: System and Circuits, Third Edition, PHI.
6. J. P. Uyemura, CMOS Logic Circuit Design, Kluwer