GUJARAT TECHNOLOGICAL UNIVERSITY

M.E Semester: 1

Communication Engineering

Subject Name: **ASIC Design**

Sr.No	Course content
1	ASIC Design flow, Design Methodotogies, Introduction to Hardware Description Language (VHDL): Stuctural, Behavioral, Data flow modeling, Concurrent and sequential VHDL, RAM and ROM, Test Benches, Finite State Machines, RTL Synthesis Test Methodology
2	Programmable Logic Design, Basics of Programmable logic devices, CPLD Architecture and its building blocks, FPGA Architectures and its building blocks, Technology mapping for FPGAs
3	Design implementation using CPLD and FPGA, Floor planning and Placement

Reference Books:

1. D.Perry, BHDL,2nd Ed., McGraw Hill International.
2. J. Bhasker, BHDL, Primer, Pearson Education Asia, Low Price Edition
3. Charles H Roth, Jr., Digital Systems Design Using VHDL, Brooks/Cole Thompson Learning
4. Z. Navabi, VHDL: Analysis and Modeling of Digital Systems, McGraw Hill International Editions
5. Michael John Sebastian Smith, Application Specific Integrated Circuits, Pearson Education Asia.
6. Xilinx and Altera Application Notes on the architecture of FPGAs and CPLDs.