GUJARAT TECHNOLOGICAL UNIVERSITY (GTU)

Competency-focused Outcome-based Green Curriculum-2021 (COGC-2021)
Semester-III

Course Title: Digital Electronics
(Course Code: 4332402)

Diploma programmer in which this course is offered	Semester in which offered
Power Electronics	Third

1. RATIONALE

The aim of introducing this course on digital electronics to impart knowledge of basic building blocks of digital logic circuits. This will enable the student to become aware of various number systems, logic gates and logic families, combinational and sequential logic circuits, which is the foundation for understanding the digital controls, microprocessors and computer systems. Through this course the student will be able to apply the same in almost all areas of electronic control and develop the testing skills.

2. COMPETENCY

The purpose of this course is to help the student to attain the following industry identified competency through various teaching learning experiences:

- **Test digital logic circuits.**

3. COURSE OUTCOMES (COs)

The practical exercises, the underpinning knowledge and the relevant soft skills associated with this competency are to be developed in the student to display the following COs:

1. **Use number systems for requirements in digital circuits.**
2. **Implement simplified Boolean equations using logic gates.**
3. **Test different types of combinational logic circuits.**
4. **Test different types of sequential logic circuits.**
5. **Classify logic families.**

4. TEACHING AND EXAMINATION SCHEME

Teaching Scheme (In Hours)			Total Credits (L+T+P/2)	Examination Scheme				
				Theory Marks		Practical Marks		Total Marks
L	T	P	C	CA	ESE	CA	ESE	
4	-	2	5	30	70	25	25	150

(*): For this practical only course, 25 marks under the practical CA has two components i.e. the assessment of micro-project, which will be done out of 10 marks and the remaining 15 marks are for the assessment of practical. This is designed to facilitate attainment of COs holistically, as there is no theory ESE.

***Legends: L**-Lecture; **T** – Tutorial/Teacher Guided Theory Practice; **P** -Practical; **C** – Credit, **CA** - Continuous Assessment; **ESE** -End Semester Examination.*

5. SUGGESTED PRACTICAL EXERCISES

*Following practical outcomes (PrOs) that are thesub-components of the Course Outcomes (Cos). Some of the **PrOs** marked **'*'** are compulsory, as they are crucial for that particular CO at the 'Precision Level' of Dave's Taxonomy related to 'Psychomotor Domain'.*

S. No.	Practical Outcomes (PrOs)	Unit No.	Approx. Hrs. required
1.	Study various number system.	1	2*
2.	Build/Test the basic logic gates (AND, OR and NOT).	2	2*
3.	Build/Test the EX-OR, EX-NOR logic gates.	2	2
4.	Build/Test NAND and NOR as universal gate.	2	2
5.	Test the De- Morgan's theorem.	2	2*
6.	Build/Test half adder circuit using EX-OR, AND, OR gates.	3	2*
7.	Build/Test full adder circuit using EX-OR, AND, OR gates.	3	2*
8.	Build/Test half subtractor circuit using EX-OR, AND, OR gates.	3	2*
9.	Build/Test full subtractor circuit using EX-OR, AND, OR gates.	3	2
10.	Build/Test the 2 to 4, 3 to 8, and 4 to 16 lines decoder circuit.	3	4
11.	Design the 4 to 16 lines decoder using 2 to 4 line decoder circuit.	3	4*
12.	Build/Test the encoder circuit.	3	2
13.	Build/Test the comparator circuit.	3	2
14.	Build/Test the parity generator, parity checker circuit.	3	2*
15.	Build/Test the 2:1, 4:1, 8:1, 16:1 multiplexer circuit.	3	4*
16.	Build/Test the 1: 2, 1:4, 1:8, and 1:16 de multiplexer circuit.	3	4
17.	Build/Test SR flip-flop.	4	2*
18.	Build/Test D flip-flop.	4	2
19.	Build/Test JK flip-flop.	4	2*
20.	Build/Test JK master slave flip-flop.	4	2
21.	Build/Test T flip-flop.	4	2
22.	To study various Logic Family Parameters.	5	2*
		Total	**28**

Note

*i. More **Practical Exercises** can be designed and offered by the respective course teacher to develop the industry relevant skills/outcomes to match the COs. The above table is only a suggestive list.*

*ii. The following are some **sample** 'Process' and 'Product' related skills (more may be added/deleted depending on the course) that occur in the above listed **Practical Exercises** of this course required which are embedded in the COs and ultimately the competency.*

S. No.	Sample Performance Indicators for the PrOs	Weightage in %
1	Prepare of experimental setup	20
2	Operate the equipment setup or circuit	20
3	Follow safe practices measures	10
4	Record observations correctly	20
5	Interpret the result and conclude	30

S. No.	Sample Performance Indicators for the PrOs	Weightage in %
	Total	**100**

6. MAJOR EQUIPMENT/ INSTRUMENTS REQUIRED

These major equipment with broad specifications for the PrOs is a guide to procure them by the administrators to user in uniformity of practical's in all institutions across the state.

S. No.	Equipment Name with Broad Specifications	PrO. No.
1	**Digital Electronics Trainer** Trainer should have Features of Logic symbol/ Schematic Diagram indicated on board mimic, On Board DC Power Supplies, Onboard Pulse Generator (TTL), Pulser Switches, 8-bit Data Switches (TTL), 8-bit bicolor LED display, Logic Probe, BCD to seven segment display, ZIF Sockets, Pullup Resistors Scope of Learning:Test the performance of Logic AND, OR, NOT, NAND, NOR, RS Flip-flop, JK Flip-flop, D Flip-flop and verify its Truth table. Study of Logic algebra. Study the application of logic gate circuit. Study the implementation of simple logic design. Test the performance of digital combinational logic circuits. Study the application of D Flip-flops as Shift Register. Study the application of JK Flip-flops as Up-Down Counter Technical Specifications: DC Power Supplies: + 5V, 1A; +3V to +15V, 500 mA (variable)- 3V to -15V, 500 mA (variable) Pulse Generator: 1Hz to 1MHz in 6 steps (Variable in between the steps) Amplitude: 5V (TTL)Duty Cycle:50 %, TTL output Mains:230V AC ±10%	2 to 9 and 17 to 19
2	**Digital Work Station** The Trainer should have Feature of Graphical LCD to show the menu of experiment and gate level diagram for selected experiment, Solderless breadboard, On Board DC Power Supply, On board Pulse Generator. Scope of Learning: Test the performance of Not gate, OR gate & AND gate, Universal gate, NAND Gate, XOR and XNOR gate, NOT Gate Using NAND Gate, OR Gate Using NAND Gate, AND Gate Using NAND Gate, AND-OR Gate, AND-NOR Gate, NAND-OR Gate, NAND-NOR Gate, NAND-NAND Gate, NOR-NOR Gate, Half Adder, Full Adder, Half Subtractor, Full Subtractor, 4-1 MUX, 1-4 DMUX, 4-2 Encoder. Technical Specification: DC Supply : +5 V, 500 mA Clock Frequency : 1 Hz, 100 Hz, 1 KHz, 100 KHz Amplitude : 3.3V (TTL) Duty cycle : 50 %, TTL output, Main Supply: 100V - 240V AC, 50/60Hz	2 to 16
3	**Flip Flop Trainer** Trainer Should have Features of Adaptable illustration of Flip-Flops, +5V SMPS Adaptor provided with the trainer for power supply. Scope of Learning: Study of S-R, J-K, D and T Flip-Flop and to verify their Transition table. Input:+5V DCLogic levels +5V:HIGH(Logic 1)0V:LOW (Logic 0) Main Supply: 100V - 240V AC, 50/60Hz	17 to 21

S. No.	Equipment Name with Broad Specifications	PrO. No.
4	**4½ Digit Multimeter** Function Range and Resolution Basic Accuracy DC volts, AC volts: 50.000 mV,500.00 mV, 5.0000 V, 50.000 V, 500.00 V, 1000.0 V. Accuracy: 0.025 %, 0.4 % (true-rms) DC current, AC current: 500.00 µA, 5000.0 µA, 50.000 mA, 400.00 mA, 5.0000 A, 10.000 A, Accuracy: 0.15 %, 0.7 % (true-rms) Temperature: -200.0 °C to 1350.0 °C (-328.0°F to 2462.0°F) Accuracy:1.0 % Resistance 50.000 Ω, 500.00 Ω, 5.0000 kΩ, 50.000 kΩ, 500.00 kΩ, 5.0000 MΩ, 50.00 MΩ, 500.0 MΩ, Accuracy: 0.05 % Capacitance 1.000 nF,10.00 nF 100.0 nF, 1.000 µF, 10.00 µF, 100.0 µF, 1000 µF, 10.00 mF, 100.0 mF, Accuracy: 1.0 % Frequency 99.999 Hz, 999.99 Hz, 9.9999 kHz, 99.999 kHz, 999.99 kHz. Accuracy: .005 %	2-21

7. AFFECTIVE DOMAIN OUTCOMES

The following ***sample*** Affective Domain Outcomes (ADOs) are embedded in many of the above mentioned COs and PrOs. More could be added to fulfill the development of this competency.

a) Work as a leader/a team member.
b) Follow safety practices while using electrical instruments and tools.
c) Realize importance of sensors and transducers in electronic circuits.

The ADOs are best developed through the laboratory/field-based exercises. Moreover, the level of achievement of the ADOs according to Krathwohl's 'Affective Domain Taxonomy' should gradually increase as planned below:

i. 'Valuing Level' in 1st year
ii. 'Organization Level' in 2nd year.
iii. 'Characterization Level' in 3rd year.

8. UNDERPINNING THEORY

Only the major Underpinning Theory is formulated as higher level UOs of *Revised Bloom's taxonomy* in order development of the COs and competency is not missed out by the students and teachers. If required, more such higher level UOs could be included by the course teacher to focus on attainment of COs and competency.

Unit	Unit Outcomes (UOs) (4 to 6 UOs at Application and above level)	Topics and Sub-topics
Unit – I Number System and Binary Codes	1a. Explain different types of numbering systems. 1b. Convert binary to decimal, octal, hexadecimal and vice-versa. 1c. Perform binary complement operations.	1.1 Number System: Binary, Octal, Decimal, Hexadecimal 1.2 Number Conversion: Binary to Decimal, Decimal to Binary, Binary to Hexadecimal, Hexadecimal to Binary, Octal to Hexadecimal and Hexadecimal to Octal. 1.3 Complements: 1's Complement, 2's Complement

Unit	Unit Outcomes (UOs) (4 to 6 UOs at Application and above level)	Topics and Sub-topics
	1d. Explain Signed and Unsinged Number system. 1e. Describe weighted and un-weighted codes and their uses.	1.4 Signed and Unsigned Binary Numbers: Unsigned, Sign Magnitude, Range. 1.5 Binary Codes: Weighted Codes, Non weighed codes, Gray Code, BCD Code.
Unit– II Boolean Algebra and Functions	2.a Simplify expression using truth table for various Gates. 2.b Apply laws of Boolean Algebra. 2.c Simplify Boolean expressions using various methods.	2.1 Logic Gates: AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR. 2.2 Boolean Algebra: Postulates, Laws, Duality Theorem, De-Morgan's Theorems, Boolean Expression and functions. 2.3 Representation of Logic Expression: SOP, POS. 2.4 Drawback of algebraic method of Simplification. 2.5 K-Map Representation: SOP, POS; simplification. 2.6 Drawback of K-Map 2.7 K-Map using Don't care condition 2.8 NAND and NOR Implementation
Unit– III Combinational Logic Circuits	3a. Classify Combinational Circuits. 3b. Explain Working of various combinational circuits using Truth Table, Logic Circuits and Simplify Boolean Expression.	3.1 Combinational Circuits: Classification, Half Adder, Full Adder, Half Subtractor, Full Subtractor,1-bit Magnitude comparator, Multiplexers (2:1,4:1, 8:1), Demultiplexers (1:2, 1:4, 1:8), Decoder (2:4, 3:8) and Encoder (Octal to Binary).
Unit– IV Sequential Logic circuits	4a. Explain Basics of Sequential Circuit. 4b. Explain Working of S - R (NOR, NAND) and D Latches using Truth Table, Logic Circuits and Simplification of Boolean Expression. 4c. Differentiate Latches and Flip Flop. 4d. Explain Working of S – R, D, J – K and T Flip Flops using Truth Table, Logic Circuits and Simplification of Boolean Expression.	4.1 Sequential Circuit: Definition, Block Diagram. 4.2 Latches: S - R (NOR, NAND) and D. 4.3 Flip Flops: S – R, D, J – K and T.
Unit– V Basics of Logic Families	5a. Classify logic Families. 5b. Explain Positive and Negative Edge Logic. 5c. Define various logic family parameters. 5d. Compare parameters of TTL and CMOS family with respect to Basic Gate, Power dissipation, Fan In, Fan	5.1 Logic Families: Classification, Positive & Negative Logic. 5.2 Logic Family Terms: Voltage Levels, Current Levels, Fan in, Fan out, Noise margin, Propagation delay, Power dissipation and Figure of merit. 5.3 Comparison of TTL and CMOS.

Unit	Unit Outcomes (UOs) (4 to 6 UOs at Application and above level)	Topics and Sub-topics
	Out, Propagation Delay and Lo-Hi Voltage Levels.	

***Note**: The UOs need to be formulated at an 'Application Level' and above of Revised Bloom's Taxonomy' to accelerate the attainment of the COs and the competency.*

9. SUGGESTED SPECIFICATION TABLE FOR QUESTIONPAPER DESIGN

Unit No.	Unit Title	Teaching Hours	Distribution of Theory Marks			
			R Level	U Level	A Level	Total Marks
I.	**Number System and Binary Codes**	12	6	2	0	15
II.	**Boolean Algebra and Functions**	14	6	8	3	17
III.	**Combinational Logic Circuits**	14	6	10	2	18
IV.	**Sequential Logic circuits**	10	8	5	0	13
V.	**Basics of Logic Families**	06	4	3	0	07

***Legends:** R=Remember, U=Understand, A=Apply and above (Revised Bloom's taxonomy)*
***Note**: This specification table provides general guidelines to assist student for their learning and to teachers to teach and question paper designers/setters to formulate test items/questions assess the attainment of the UOs. The actual distribution of marks at different taxonomy levels (of R, U and A) in the question paper may vary slightly from above table.*

10. SUGGESTED STUDENT ACTIVITIES

Other than the classroom and laboratory learning, following are the suggested student-related ***co-curricular*** activities which can be undertaken to accelerate the attainment of the various outcomes in this course: Students should conduct following activities in group and prepare reports of about 5 pages for each activity, also collect/record physical evidences for their (student's) portfolio which will be useful for their placement interviews:

a) Compare and analyze any two Digital IC Datasheets.
b) Observe the output parameter as well waveform using simulation and compare it with practical results.
c) Prepare Hazard Analysis report for various materials used in Digital ICs.
d) Use Digital ICs for Logic Design Implementation.

11. SUGGESTED SPECIAL INSTRUCTIONAL STRATEGIES (if any)

These are sample strategies, which the teacher can use to accelerate the attainment of the various outcomes in this course:

a) Massive open online courses (***MOOCs***) may be used to teach various topics/sub topics.
b) Guide student(s) in undertaking micro-projects.
c) ***'L' in section No. 4***means different types of teaching methods that are to be employed by teachers to develop the outcomes.

d) About ***20% of the topics/sub-topics*** which are relatively simpler or descriptive in nature is to be given to the students for ***self-learning***, but to be assessed using different assessment methods.
e) With respect to ***section No.10***, teachers need to ensure to create opportunities and provisions for ***co-curricular activities***.
f) Use video/animation films to demonstrate various Digital Circuits.
g) Guide students for reading data sheets.

12. SUGGESTED MICRO-PROJECTS

Only one micro-project is planned to be undertaken by a student that needs to be assigned to him/her in the beginning of the semester. In the first four semesters, the micro-project is group-based. However, in the fifth and sixth semesters, it should be preferably be ***individually*** undertaken to build up the skill and confidence in every student to become problem solver so that s/he contributes to the projects of the industry. In special situations where groups have to be formed for micro-projects, the number of students in the group should ***not exceed three.***

The micro-project could be industry application based, internet-based, workshop-based, laboratory-based or field-based. Each micro-project should encompass two or more COs which are in fact, an integration of PrOs, UOs and ADOs. Each student will have to maintain dated work diary consisting of individual contribution in the project work and give a seminar presentation of it before submission. The total duration of the micro-project should not be less than ***16 (sixteen) student engagement hours*** during the course. The student ought to submit micro-project by the end of the semester to develop the industry oriented COs.

A suggestive list of micro-projects is given here. This has to match the competency and the COs. Similar micro-projects could be added by the concerned course teacher:

a) Make universal test board for Digital Circuits to verify different Gates and Combinational Circuits.
b) Make a project to perform operation of decimal calculator using digital Gates and ICs.

13. SUGGESTED LEARNING RESOURCES

S. No.	Title of Book	Author	Publication with place, year and ISBN
1	Digital Electronics and Logic Design	Dr. Sharma Sanjay	S. K. Kataria & Sons, ISBN 978-93-5014-199-1
2	Digital Logic and Computer Design	M. Morris Mano	Pearson Education India, ISBN-10: 933254252X
3	Fundamentals of Digital Circuits	A. Anand Kumar	PHI Learning, ISBN-10: 8120352688
4	Digital Fundaments	Floyd Thomas	Pearson Education India, ISBN 10: 1-292-07598-8
5	Digital Electronics Principles, Devices and Applications	Anil K. Maini	John Wiley & Sons Ltd, ISBN 978-0-470-03214-5

14. SOFTWARE/LEARNING WEBSITES

a) https://www.geeksforgeeks.org/digital-electronics-logic-design-tutorials/
b) https://www.tutorialspoint.com/digital_circuits/index.htm
c) https://www.electronics-tutorials.ws/logic/logic_1.html
d) https://www.youtube.com/watch?v=M0mx8S05v60&list=PLBlnK6fEyqRjMH3mWf6kwqiTbT798eAOm
e) https://www.youtube.com/watch?v=8V5HdgcG-Aw&list=PL8PvmC2cEsGTqrz0whJJb_If4l8jPrp9F
f) https://www.youtube.com/watch?v=DBTna2ydmC0&list=PLwjK_iyK4LLBC_so3odA64E2MLgIRKafl
g) https://www.youtube.com/watch?v=4IoP0BS5Usc&list=PLf6hLBoZhgD7uANVx53UbvmRtUykLHQtx&index=19
h) https://www.youtube.com/watch?v=vsoYlH1_hbc&list=PLWPirh4EWFpHk70zwYoHu87uVsCC8E2S-
i) https://nptel.ac.in/courses/108105132
j) https://www.youtube.com/watch?v=M0mx8S05v60&list=PLBlnK6fEyqRjMH3mWf6kwqiTbT798eAOm

15. PO-COMPETENCY-CO MAPPING

Semester III	Digital Electronics (Course Code: 4332402)						
	POs and PSOs						
Competency & Course Outcomes	PO 1 Basic & Discipline specific knowledge	PO 2 Problem Analysis	PO 3 Design/ development of solutions	PO 4 Engineering Tools, Experimentation &Testing	PO 5 Engineering practices for society, sustainability & environment	PO 6 Project Management	PO 7 Life-long learning
Competency	Select specific sensors and transducers in electronic circuits.						
Course Outcomes							
CO 1) Use number systems for requirements in digital circuits.	2	1	1	0	1	1	1
CO 2) Implement simplified Boolean equations using logic gates.	2	1	2	2	1	1	2
CO 3) Test different types of combinational logic circuits.	2	1	2	2	1	2	3
CO 4) Test different types of sequential logic circuits.	2	1	2	2	1	2	2
CO 5) Classify logic families.	2	1	2	1	1	1	3

Legend: '**3**' for high, '**2**' for medium, '**1**' for low or '**-**' for the relevant correlation of each competency, CO, with PO/ PSO

16. COURSE CURRICULUM DEVELOPMENT COMMITTEE

GTU Resource Persons

S. No.	Name and Designation	Institute	Contact No.	Email
1.	Mr. Sunil A. Patel, Lecturer in Power Electronics	Dr. S. & S. S. Ghandhy College of Engineering & Technology, Surat	+91- 9898073753	Patel_sunil5@gtu.edu.in