GUJARAT TECHNOLOGICAL UNIVERSITY

Master of Engineering
Subject Code: 3735406
Semester – III
Subject Name: SoC Design

Type of course: Core-II

Prerequisite: Digital Circuit Design, Embedded System, VLSI Design

Rationale: This course is essential for understanding ASIC Design, Front-End Simulation, Synthesis of behavioral design, Low power chip design concepts.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks				Total Marks
				Theory Marks		Practical Marks		
L	T	P	C	ESE (E)	PA (M)	ESE (V)	PA (I)	
2	0	2	3	70	30	30	20	150

Content:

Sr. No.	Content	Total Hrs
1	**Unit 1: ASIC** Overview of ASIC types, design strategies, CISC, RISC & NISC approaches for SOC architectural issues & its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.	8
2	**Unit 2: NISC** NISC Control Words methodology, NISC Applications & Advantages, Architecture Description Languages (ADL) for design & verification of Application Specific Instruction set Processes(ASIP), No Instruction Set Computer(NISC) design flow, modeling NISC architectures and systems, use of Generic Netlist Representation – A formal language for specification, compilation & synthesis of embedded processors.	7
3	**Unit 3: Simulation** Different simulation modes, behavioral, functional, static timing , gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design & control logic, Minimization of interconnects impact, clock tree design issues.	8
4	**Unit 4: Low power SoC design/Digital system**	8

	Design Synergy, Low power system perspective - power gating, clock gating, adaptive voltage scaling(AVS), Static voltage scaling, Dynamic clock frequency & voltage scaling(DCFS), building block optimization, building block memory, power down techniques, power consumption verification.	
5	**Unit 5: Synthesis** Role & Concept of graph theory & its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal & admittance graph, Technology independent & technology dependent approaches of synthesis, optimization constraints, Synthesis report analysis Single core & Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs.	**7**
6	**Unit 6:** Case study for overview of cellular phone design with emphasis on area optimization, speed improvement & power minimization.	**2**

Reference Books:

- Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication". Cambridge University Press,2008
- B. Al Hashimi, "System on Chip-Next Generation Electronics", The IET, 2006
- Rochit Rajsuman, "System-on-a-chip: Design and Test", Advantest America R&D Center,2000
- P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann, 2008
- Michacl J. Flynn and Waync Luk, "Computer System Design : System on Chip:, Wilcy 2011

Course Outcomes:

Sr. No.	CO statement	Marks % weightage
CO-1	Design SoC based System for engineering applications	30
CO-2	Analyse given problem in the framework of SoC based Design approaches.	40
CO-3	Understand • SoC Design and its impact on electronics design philosophy and Microelectronics. • Synthesis of behavioural design with different construct. • Low power SoC design methods.	30

List of Experiments:

- Understand NIOS Processor in Quartus-II
- Design and implement complex SoC including NIOS processor, Memory, I/O.
- Design and implement complex SoC including NIOS processor and communication peripherals (UART, I2C, SPI, VGA, HDMI etc)
- Understand MicroBlaze Processor in Xilinx ISE.
- Design and implement complex SoC includin MicroBlaze Processor, Memory, I/O.
- Design and implement complex SoC including MicroBlaze Processor and communication peripherals (UART, I2C, SPI, VGA, HDMI etc)
- Simulate Power gating techniques using NGSpice/PSPICE.
- Simulate adaptive voltage scaling techniques for CMOS Design using NGSpice/PSPICE.

Major Equipment:

- NGSpice / Pspice Tool
- Altera Quartus-II
- Xilinx ISE
- DE1/DE2 Development board (Cyclone-II/III FPGA) From Altera
- Spartan-6 Development board From Xilinx

List of Open Source Software/learning website:

- NPTEL / Coursera Videos
- NGSPICE / PSPICE