GUJARAT TECHNOLOGICAL UNIVERSITY

Subject Name: Verification Methodology (Elective)
Subject Code: 3735203

Semester III

Type of course: ME - Electronics & Communication Engineering (VLSI & Embedded Systems Design)

Prerequisite: Understanding of system Verilog concepts, C programming, OOPS concepts

Rationale: NA

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks				Total Marks
L	T	P	C	Theory Marks		Practical Marks		
				ESE (E)	PA (M)	PA (V) ESE	PA (I)	
4	2#	0	5	70	30	30	20	150

L- Lectures; T- Tutorial/Teacher Guided Student Activity; P- Practical; C- Credit; ESE- End Semester Examination; PA- Progressive Assessment;

Content:

Sr. No.	Content	Total Hrs	% Weightage
1	**Verification Using System Verilog** What is the Functional Verification, What is the Assertion based Verification, Why use System Verilog for Verification, OOP concept for System Verilog, Layered approach for Verification, Designing with OOP, OOP classes, OOP connections, Block level testing using OOP, Chip Level Testing, Functional Coverage, Assertion Based verification, Interfacing with C	6	10
2	**Universal Verification Methodology Understanding** Verification Component Overview, Transaction Level Modeling (TLM), Developing Reusable Verification Component, Using Verification component, Using Register Layer Class	6	10
3	**Low Power Verification Techniques (CPF/UPF)** Need of Power Aware Simulation, Understanding Unified Power Format file, Writing CPF/UPF, Assertions checking for the low power Simulation	6	10
4	**Verification of SOC with ARM/MIPS Processor** ARM architecture as covered in Embedded classes, Development of ARM/MIPS BFM. Writing C test case on ARM, Using ARMCC and ARMSS compiler and linking it with simulator	7	20
5	**Verification Environment build and Automation.** Use of Make file, Perl & TCL script in running the test, Running Regression of the test suit for the Device Under test, Automatic regression results generation, Merging of the code & functional coverage, Ranking of the test suit.	7	20

Reference Books:

1. System Verilog LRM
2. Hardware Verification with System Verilog- Mike Mintz & Robert Ekendahl System Verilog for Verification – Chris Spear
3. UVM user Manual

Course Outcome:

After learning the course the students should be able to:

1. Understand about the basics of data types, assertions, constraint driven and oops concepts.
2. Able to write test environment using system Verilog.
3. Understand about the OVM and UVM verification methodology.

List of Experiments: (with Open Ended Problems)

1. Wirte a system verilog test environment for synchronous FIFO.
2. Wirte a system verilog test environment for asynchronous FIFO.
3. Design all the combinational and sequential circuit using system Verilog.

List of Open Source Software/learning website:

1. Mentor graphics

Review Presentation (RP): The concerned faculty member shall provide the list of peer reviewed Journals and Tier-I and Tier-II Conferences relating to the subject (or relating to the area of thesis for seminar) to the students in the beginning of the semester. The same list will be uploaded on GTU website during the first two weeks of the start of the semester. Every student or a group of students shall critically study 2 papers, integrate the details and make presentation in the last two weeks of the semester. The GTU marks entry portal will allow entry of marks only after uploading of the best 3 presentations. A unique id number will be generated only after uploading the presentations. Thereafter the entry of marks will be allowed. The best 3 presentations of each college will be uploaded on GTU website