GUJARAT TECHNOLOGICAL UNIVERSITY

Subject Name: Standard Cell Library and Memory Design (Elective)
Subject Code: 3735202

Semester III

Type of course: ME - Electronics & Communication Engineering (VLSI & Embedded Systems Design)

Prerequisite: Basic of computer organization.

Rationale: NA

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks				Total Marks
L	T	P	C	Theory Marks		Practical Marks		
				ESE (E)	PA (M)	PA (V) ESE	PA (I)	
4	2#	0	5	70	30	30	20	150

L- Lectures; T- Tutorial/Teacher Guided Student Activity; P- Practical; C- Credit; ESE- End Semester Examination; PA- Progressive Assessment;

Content:

Sr. No.	Content	Total Hrs	% Weightage
1	**Introduction** IC design flows. Use of standard cell elements vs. custom design and Gate array paradigms. Introduction to memory types and construction of memory elements.	6	10
2	**Standard cell library composition and usage** Types of standard cell elements. Logical and functional elements, primitives and complex macros. Sequential elements and register files. (Flip flop and latch design). Data path elements. Library size vs. usage in standard flows. Drive strength and cell families. Layout of library elements – single height, double height cells. Power Management cells.	6	10
3	**Standard cell characterization** Usage of standard cells by various tools. Information needed at each stage of design flow. Characterization parameters, setup and runs across PVT corners. Library representation formats. (Gate level simulation, synthesis, timing, layout, timing, LVS, DRC)	6	10
4	**Memory elements and array design** Volatile and Non-volatile RAM, ROM, EPROM, Flash (EEPROM), OTP elements and cell design. State retention volatile memories. Array design – architecture, bitline/wordline optimization, sense-amps and mux/demux architecture. Memory banking, refresh cycle management. Multi-port memories. Cache memories. Special memories such as CAMs.	**7**	20
5	**Memory defects, failures and testing, layout and characterization** Memory defects and repair. Temporal failures, Soft errors, Membist and other test techniques for memories. Memory layout and its impact on performance. Characterization of memories – timing, area, power parameters. Layout views	7	20

	– hard macro representation, keep outs and congestion impact.		

Reference Books:

Standard cell and memory library documentation by Vendors 90nm EDK library

Course Outcome:

After learning the course the students should be able to:

- Analyse the IC design flows and memory element types and their construction.
- Evaluate the standard cell library and its types and study about the data path elements.
- Understand about the usage of standard cells and library representation formats.
- Analyse the working of different types of memory elements and their architecture.
- Evaluate the defects in memory, their failures and testing.

List of Experiments: (with Open Ended Problems)

1. Study and implementation of performance of memory systems and their impact on system performance
2. Study and implementation of Standard interfaces

List of Open Source Software/learning website:

1. **Linux**
2. **Perl**
3. **Gcc**
4. **Gdb**
5. **VCS**

Review Presentation (RP): The concerned faculty member shall provide the list of peer reviewed Journals and Tier-I and Tier-II Conferences relating to the subject (or relating to the area of thesis for seminar) to the students in the beginning of the semester. The same list will be uploaded on GTU website during the first two weeks of the start of the semester. Every student or a group of students shall critically study 2 papers, integrate the details and make presentation in the last two weeks of the semester. The GTU marks entry portal will allow entry of marks only after uploading of the best 3 presentations. A unique id number will be generated only after uploading the presentations. Thereafter the entry of marks will be allowed. The best 3 presentations of each college will be uploaded on GTU website