GUJARAT TECHNOLOGICAL UNIVERSITY

Subject Name: Design for Testability (Elective)
Subject Code: 3735201

Semester III

Type of course: ME - Electronics & Communication Engineering (VLSI & Embedded Systems Design)

Prerequisite: VLSI Basics and concepts.

Rationale: NA

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks				Total Marks
L	T	P	C	Theory Marks		Practical Marks		
				ESE (E)	PA (M)	PA (V) ESE	PA (I)	
4	2#	0	5	70	30	30	20	150

L- Lectures; T- Tutorial/Teacher Guided Student Activity; P- Practical; C- Credit; ESE- End Semester Examination; PA- Progressive Assessment;

Content:

Sr. No.	Content	Total Hrs	% Weightage
1	Introduction: The need for testing, Fabrication, Assembly and Test Process Flows.	7	15
2	Scan Testing: Using additional primary inputs and outputs to improve controllability and observability, Scan-based testing. Design rules, Ways to overcome rule violations. Automated Test Pattern Generation for scan testing. Scan test protocol, Full-scan and partial scan, Automated scan design systems, Scan design flow, Scan design overhead: area, timing, power considerations.	7	15
3	Built-in self-testing (BIST): BIST architecture, Test compression methods, Random and weighted random pattern testability, BIST Pattern generator and response analyzer, Theory of Linear feedback shift registers (LFSR), Generating test vectors and Signature analysis, Scan-based BIST architecture, Built-in Logic Block Observation (BILBO), Test point insertion for improving random testability, Memory IC BIST and Built-In self-repair.	8	20
4	Boundary Scan Testing: Boundary scan technique. JTAG standard (IEEE 1149.1), Application of Boundary scan for PCB testing, Boundary scan instructions, Boundary Scan Description Language (BCDL), Boundary scan Test access port (TAP), TAP controller, Boundary scan instructions, Instruction register, Test data register. Boundary scan register, TAP controller state diagram, Testable design flow, Using Boundary scan TAP for IC internal circuit testing.	8	20

Reference Books:

1. B. Friedman. Digital Systems Testing and Testable Design. Jaico Publishing House. 2005. 670p.
2. M. L. Bushnell and V. D. Agrawal. Essentials of Electronic Testing, Kluwer Academic Publishers, 2000, 709p.
3. M. Abramovici, M.A. Breuer, A.D. Friedman. Digital Systems Testing and Testable Designs. 1998.
4. Neil H.E. Waste, K. Eshraghian. Principles of CMOS VLSI Design. Addison Wesley; 2nd edition, 1994. 735p.

Course Outcome:

After learning the course the students should be able to:

1. Understand the need of testing, fabrication and assembly of VLSI Circuits.
2. Analyse about the scan based techniques for testing of VLSI Circuits based.
3. Understand about the BIST and its architecture, pattern generator and BILBO for VLSI testing.
4. Understand the design for testability and adhoc design in detail.
5. Analyse the BIST testing and its architecture along with BILBO and scan based BIST architecture.

Review Presentation (RP): The concerned faculty member shall provide the list of peer reviewed Journals and Tier-I and Tier-II Conferences relating to the subject (or relating to the area of thesis for seminar) to the students in the beginning of the semester. The same list will be uploaded on GTU website during the first two weeks of the start of the semester. Every student or a group of students shall critically study 2 papers, integrate the details and make presentation in the last two weeks of the semester. The GTU marks entry portal will allow entry of marks only after uploading of the best 3 presentations. A unique id number will be generated only after uploading the presentations. Thereafter the entry of marks will be allowed. The best 3 presentations of each college will be uploaded on GTU website