GUJARAT TECHNOLOGICAL UNIVERSITY

Master of Engineering
Subject Code: 3732605
Semester – III
Subject Name: VLSI Test Principles and Architecture

Type of course: Introductory course for VLSI testing

Prerequisite: Nil

Rationale: This course provides a platform for students to understand importance of testing, fundamental VLSI test principles, basic concepts of design of testability (DFT), logic simulation and fault simulation, various techniques for test pattern generation and various logic BIST techniques, etc.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks				Total Marks
				Theory Marks		Practical Marks		
L	T	P	C	ESE (E)	PA (M)	ESE (V)	PA (I)	
3	0	0	3	70	30	0	0	100

Content:

Sr No	Course Content	Teaching Hours
1	**Introduction:** Importance of Testing, Testing during VLSI Lifecycle, Challenges in VLSI Testing, Levels of Abstraction in VLSI Testing, Historical Review of VLSI Test Technology.	**7**
2	**Design and Testability:** Introduction, Testability Analysis, Design for Testability Basics, Scan Cell Designs, Scan Architectures, Scan Design Rules, Scan Design Flow, Special purpose Scan Designs, RTL Design for Testability.	**10**
3	**Logic and Fault Simulation:** Introduction, Simulation Models, Logic Simulation, Fault Simulation	**7**
4	**Test Generation:** Introduction, Random Test Generation, Theoretical Background: Boolean Difference, designing a Stuck-At ATPG for Combinational Circuits, Designing a Sequential ATPG, Untestable Fault Identification.	**9**
5	**Logic Built-In Self-Test:** Introduction, BIST Design Rule, Test Pattern Generation, Output Response Analysis, Logic BIST Architectures, Fault Coverage Enhancement	**9**
Total		**42**

Distribution of Theory Marks					
R Level	U Level	A Level	N Level	E Level	C Level
10	**30**	**20**	**20**	**10**	**10**

Legends: R: Remembrance; U: Understanding; A: Application, N: Analyze and E: Evaluate C: Create and above Levels (Revised Bloom's Taxonomy)

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Reference Books:

1. VLSI Test Principles and Architectures, Wang Wu Wen, Morgan Kaufmann Publishers,2011
2. Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", M. Bushnell and V. D. Agrawal, Kluwer Academic Publishers, 2000
3. Digital Systems Testing and Testable Design, M. Abramovici, M. A. Breuer and A. D. Friedman, IEEE Press, 1990
4. Introduction to Formal Hardware Verification, T.Kropf, Springer Verlag, 2000
5. System-on-a-Chip Verification- Methodology and Techniques, P. Rashinkar, Paterson and L. Singh, Kluwer Academic Publishers, 2001

Course Outcome:

Sr. No.	CO statement	Marks % weightage
CO-1	To realize importance and challenges of VLSI Testing at different abstraction levels.	10
CO-2	To study and apply various fault models for generation of test vectors and to learn various DFT techniques to improve testability of circuits.	25
CO-3	To understand and use various algorithms for test pattern generation.	15
CO-4	To perform logic and fault simulation for designing and testing of VLSI circuits.	25
CO-5	To study and analyze effect of logic built in self test (a DFT technique) in VLSI circuits designing.	25

List of Experiments:

1	Write a VHDL/Verilog code to realize functioning of Observation Point Insertion technique.
2	Write a VHDL/Verilog code to realize functioning of Control and Observation point Insertion techniques.
3	Write VHDL/Verilog code for MUX-D scan cell and Level Sensitive/edge triggered muxed-D scan cell.
4	Write a VHDL/Verilog code to realize functioning of clocked scan cell and LSSD scan cell design.
5	Write a VHDL/Verilog code to realize functioning of LSSD double latch design.
6	Write a VHDL/Verilog code to realize functioning of Mixing negative-edge and positive-edge scan cell in a scan chain.
7	Write a VHDL/Verilog code to realize functioning of Linear feedback shift register.
8	Write a VHDL/Verilog code to realize functioning of built-in logic block observer.
9	Write a VHDL/Verilog code to realize functioning of Fixing bus contention in scan design rules.
10	Write a VHDL/Verilog code to realize functioning of Adding a lock-up latch between cross-Clock-domain scan cells.

Open Ended Problems:

1	Write a C Program to calculate observability and controllability parameters of given circuit.
2	Write a C Program to generate test vectors for stuck at faults for a given combinational circuit.
3	Write a C Program to generate test vectors for transistors faults for a given circuit.
3	Write a C Program for Genetic algorithm.
4	Write a C Program for D algorithm.
5	Write a C Program for PODEM algorithm.
6	Design a one hot encoder for testing a tristate bus with four independent tristate drivers in BIST

List of Open Source Software/ Learning website:

1. ngspice/Xilinx/Dev C++ (software)
2. www.nptel.ac.in
3. www.ocw.mit.edu
4. www.mosis.com
5. www.berkeley.edu