GUJARAT TECHNOLOGICAL UNIVERSITY

Master of Engineering
Subject Code: 3732604
Semester – III
Subject Name: Low Power CMOS Circuit Design

Type of course: CMOS circuit design addressing Low power issues

Prerequisite: Basic knowledge of MOSFET, CMOS circuits

Rationale: This course provides a platform for students to analyze working of low power digital circuits and systems. This is one of the advanced courses, which will develop knowledge related to power dissipation issues in electronic systems and possible solutions to circumvent them.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks				Total Marks
L	T	P	C	Theory Marks		Practical Marks		
				ESE (E)	PA (M)	ESE (V)	PA (I)	
3	0	0	3	70	30	0	0	100

Content:

Sr. No.	Topics	Teaching Hrs.
1	**Introduction to Low Power Issues in VLSI:** Switching Power Consumption, Short – circuit Power Consumption, leakage Power Consumption, Low Power IC Design beyond Sub-20 nm Technology, Issues Related to Silicon Manufacturability and Variation, Issues Related to Design Productivity, Limitation Faced by CMOS, International Technology Roadmap for Semiconductors, Different Groups of MOSFETs, Three MOS Types, Low Leakage MOSFET, Importance of Subthreshold Slope, Why Is Subthreshold Current Exponential in Nature?, Subthreshold Leakage and Voltage Limits, Importance of Subthreshold Slope in Low Power Operation, Ultralow Voltage Operation, Low Power Analog Circuit Design, Fundamental Consequence of Lowering Supply Voltage, Analog MOS Transistor Performance Parameters.	7
2	**Scaling and Short Channel Effects in MOSFET:** MOSFET Scaling, Influence of voltage scaling on Power and Delay, VTCMOS circuits, MTCMOS circuits, Gate Oxide Scaling, Gate Leakage Current, Mobility, High-k Gate Dielectrics, Key Guidelines for Selecting an Alternative Gate Dielectric, Materials, Gate Tunneling Current, Gate Length Scaling, Introduction to Short Channel Effect in MOSFET, Reduction of Effective Threshold Voltage, Drain-induced Barrier Lowering, Mobility Degradation and Surface Scattering, Surface	10

	Scattering, Hot Carrier Effect, Punch-through Effect, Velocity Saturation Effect, Increase in Off-state Leakage Current, Lightly Doped Drain Structure, Channel Engineering Technique, Gate Engineering Technique, Single Halo Dual Material Gate MOSFET, Double Halo Dual Material Gate MOSFET, Double Gate MOSFET, Dual Material Double Gate MOSFET, Triple Material Double Gate MOSFET, FinFET, Triple Gate MOSFET, Gate-all-around MOSFET, Surrounding Gate MOSFET, Silicon Nanowires, Fringing-induced Barrier Lowering, Silicon-on-insulator MOSFETs.	
3	**Advanced Energy-reduced CMOS Inverter Design:** Introduction, Transfer Characteristics of Inverter, Static CMOS Inverter in Super-threshold Regime, Introduction to Subthreshold Logic.	6
4	**Advanced Combinational Circuit Design:** Static CMOS Logic Gate Design, Complementary Properties of CMOS Logic, Pseudo-nMOS Gates, Sizing of Transistor in CMOS Design Style, Introduction to Logical Effort, Delay Estimation by Logical Effort, Tristate Buffer, Transmission Gates and Tristates, Implementation of Combinational Circuit Using DTMOS Logic for Ultralow Power Application, ECLR Structure, Power Consumption, Propagation Delay	10
5	**Advanced Energy-reduced Sequential Circuit Design:** Basics of Regenerative Circuits, Basic SR Flip-flop/Latch, Clocked *JK* Latch, Master–slave Flip-flop, D Latch, Master–slave Edge-triggered Flip-flops, Timing Parameters for Sequential Circuits, Clock Skews due to Non-ideal Clock Signal, Design and Analysis of the Flip-flops Using DTMOS Style, Adiabatic Flip-flop	9
Total		**42**

Suggested Specification table with Marks (Theory):

Distribution of Theory Marks					
R Level	U Level	A Level	N Level	E Level	C Level
20	**30**	**20**	**10**	**10**	**10**

Legends: R: Remembrance; U: Understanding; A: Application, N: Analyze and E: Evaluate C: Create and above Levels (Revised Bloom's Taxonomy)

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Reference Books:

1. Low Power VLSI Design, Dr. Angsuman Sarkar, Prof. (Dr.) Chandan Kumar Sarkar, De Gruter Oldenbourg edition.
2. Low- Voltage, Low Power, VLSI Subsystems, Kiat-Seng Yeo ,Kaushik Roy, TATA McGraw-HILL EDITION.
3. CMOS Digital Integrated Circuits, 4th Edition, Sung-Mo Kang, Yusuf Leblebici , TATA McGraw-HILL EDITION.
4. Low-Power Cmos Vlsi Circuit Design by Kaushik Roy, Sharat C. Prasad, Willey India Edition Low-power CMOS design, Anantha P. Chandrakasan, IEEE press

Course Outcome:

Sr. No.	CO statement	Marks % weightage
CO-1	Understand basic issues in low power VLSI circuit design.	20 %
CO-2	Understand basic concepts of power consumption in CMOS circuits, techniques for the power reduction and the effects of voltage scaling on low power circuits.	20 %
CO-3	Apply concept of low power CMOS circuit techniques in combinational and sequential CMOS circuit.	30 %
CO-4	Implementation of combinational and sequential circuits using various low power techniques for ultralow power applications.	20 %
CO-5	Evaluate performance of combinational and sequential low power circuits implemented with DTMOS and adiabatic logic.	10 %

List of Experiments:

1. To obtain leakage current of MOSFET devices for following technology:
    a. 250 nm
    b. 180 nm
    c. 90 nm
2. To obtain various power dissipation components in CMOS Inverter circuit for various technologies.
3. To simulate CMOS Inverter circuit using adiabatic logic concept and obtain power dissipation.
4. To simulate CMOS NAND circuit and obtain power dissipation.
5. To simulate CMOS NOR circuit and obtain power dissipation.
6. To implement and analyze two 4 bit adder without using XOR Gate.

7. To implement and analyze XOR/XNOR gate using following method:
    A. Dual rail domino logic style
    B. DPL
8. To implement and compare full adder using different methods.
9. To implement and analyze D latch.
10. To implement and compare Power dissipation of the 2 × 2 multiplier in different frequency.

Open Ended Problems:

1. Simulate stacking effect in 2- input NOR gate.
2. Design NAND gate realization of the single-rail domino logic.
3. Design load less CMOS 4T SRAM cell using NgSpice.
4. Design ATD (Address Transition Detection) circuit using NgSpice.
5. Compare all types of sense amplifiers.
6. Design and compare 1T DRAM and SRAM using NgSpice.
7. Design two-phase back-bias generator.
8. Design and implement conventional CMOS full adder and modified CMOS full adder. Compare the speed between these two full adders.

Major Equipment: Function Generator, Power Supply, Multi-meter, Digital Storage Oscilloscope

List of Open Source Software/learning website:
Ng-spice/Multisim
LTspice
www.nptel.com
www.nptel.ac.in