GUJARAT TECHNOLOGICAL UNIVERSITY

Master of Engineering Syllabus

Subject Code : 3726301

Subject Name : VLSI Testing

WEF Academic Year :	2023 - 24
Semester :	2
Category of the Course :	Core

Prerequisite :	Basic knowledge of digital electronics.
Rationale :	This course provides a platform for students to understand importance of testing, fundamentalVLSI test principles, basic concepts of design of testability (DFT), logic simulation and fault simulation,various techniques for test pattern generation and various logic BIST techniques, etc.

Course Scheme :

Teaching Scheme			Total Credits	Assessment Pattern and Marks				Total Marks
				Theory		Practical		
L	T	PR	C	ESE (E)	PA(M)	ESE (V)	PA (I)	
3	0	2	4	70	30	20	30	150

Course Content :

Sr. No.	Course Content	No. of Hours	% of Weightage
1	**Introduction :** Importance of Testing, Testing during VLSI Lifecycle, Challenges in VLSI Testing, Levels of Abstraction in VLSI Testing, Historical Review of VLSI Test Technology.	6	9%
2	**Design and Testability :** Introduction, Testability Analysis, Design for Testability Basics, Scan Cell Designs, Scan Architectures, Scan Design Rules, Scan Design Flow, Special purpose Scan Designs, RTL Design for Testability.	10	21%
3	**Logic and Fault Simulation :** Introduction, Simulation Models, Logic Simulation, Fault Simulation.	10	20%
4	**Test Generation :** Introduction, Random Test Generation, Theoretical Background: Boolean Difference, designing a Stuck-At ATPG for Combinational Circuits, Designing a Sequential ATPG, Untestable Fault Identification, Designing a Simulation-Based ATPG, Advanced Simulation-Based ATPG, Hybrid Deterministic and Simulation-Based ATPG, ATPG for Non-Stuck-At Faults, Other Topics in test Generation.	10	25%
5	**Logic Built-In Self-Test :** Introduction, BIST Design Rule, Test Pattern Generation,Output Response Analysis, Logic BIST Architectures, Fault Coverage Enhancement,BIST Timing /Control, Design Practice.	10	25%
	Total	**46**	**100%**

Reference Book :

1. VLSI Test Principles and Architectures, Wang Wu Wen, Morgan Kaufmann Publishers.
2. Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", M. Bushnell and V. D. Agrawal, Kluwer Academic Publishers, 2000.
3. Digital Systems Testing and Testable Design, M. Abramovici, M. A. Breuer and A. D. Friedman, IEEE Press, 1990.
4. Introduction to Formal Hardware Verification, T.Kropf, Springer Verlag, 2000.
5. System-on-a-Chip Verification- Methodology and Techniques, P. Rashinkar, Paterson and L. Singh, Kluwer Academic Publishers, 2001.

Course Outcome :

After Completion of the Course, Student will able to :

No.	Course Outcomes
01	To realize importance and challenges of VLSI Testing at different abstraction levels.
02	To study and apply various fault models for generation of test vectors.
03	To calculate observability and controllability parameters of given circuit.
04	To study techniques to improve testability of a given circuit.
05	To convert a given circuit into a scan design.
06	To apply concepts of logic simulation and fault simulation in designing and testing of VLSIcircuits.
07	To apply various algorithms for test pattern generation.
08	To study and analyze effect of logic built in self-test (a DFT technique) in VLSI circuitsdesigning.

Suggested Course Practical List :

1. To develop an exhaustive testbench for lower-level combinational designs: (1) Adder (2) Subtractor(3) Multiplexer (4) Demultiplexer
2. To develop testbench for various flip-flops.
3. To develop testbench for various counters.
4. Write a HDLcode and testbench to realize functioning of Linear Feedback Shift Register (LFSR).
5. Write a HDLcode to realize functioning of Observation Point Insertion Technique.
6. Write a HDLcode to realize functioning of Control Point Insertion Technique.
7. Write HDLcode for MUX-D scan cell and Level Sensitive/Edge Triggered MUXED-D scan cell.
8. Write a HDL code to realize functioning of clocked scan cell and LSSD scan cell design.
9. Write a HDL code to realize functioning of LSSD double latch design.
10. Write a HDL code to realize functioning of mixing negative-edge and positive-edge scan cell in a scan chain.

11. Write a HDL code to realize functioning of built-in logic block observer.
12. Write a HDL code to realize functioning of 32-bit RAM.
13. Write a HDL code and testbench to implement 8 BIT ALU.
14. Write a HDL code to realize functioning of fixing bus contention in scan design rules.
15. Write a HDL code to realize functioning of Adding a lock-up latch between cross-clock-domain scan cells.

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