



GUJARAT TECHNOLOGICAL UNIVERSITY

Master of Engineering

Subject Code: 3726105

Semester – II

Subject Name: Low Power VLSI Design

Type of course: Elective

Prerequisite: NA

Rationale:

Teaching and Examination Scheme:

| Teaching Scheme | | | Credits C | Examination Marks | | | | Total Marks |
|-----------------|---|---|--------------|-------------------|--------|-----------------|----|----------------|
| L | T | P | | Theory Marks | | Practical Marks | | |
| | | | ESE(E) | PA (M) | PA (V) | PA (I) | | |
| 3 | 0 | 2 | 4 | 70 | 30 | 30 | 20 | 150 |

Content:

| Sr. No. | Content | Total Hrs |
|---------|---|--------------|
| 1 | Technology & Circuit Design Levels: Sources of power dissipation in digital ICs, degree of freedom, recurring themes in low-power, emerging low power approaches, dynamic dissipation in CMOS, effects of V _{dd} & V _t on speed, constraints on V _t reduction, transistor sizing & optimal gate oxide thickness, impact of technology scaling, technology innovations. | |
| 2 | Low Power Circuit Techniques: Power consumption in circuits, flip-flops & latches, high capacitance nodes, energy recovery, reversible pipelines, high performance approaches | |
| 3 | Low Power Clock Distribution: Power dissipation in clock distribution, single driver Versus distributed buffers, buffers & device sizing under process variations, zero skew Vs. Tolerable skew, chip & package co-design of clock network. | |
| 4 | Logic Synthesis for Low Power estimation techniques: Power minimization techniques, Low power arithmetic components- circuit design styles, adders, multipliers | |
| 5 | Low Power Memory Design: Sources & reduction of power dissipation in memory subsystem, sources of power dissipation in DRAM & SRAM, low power DRAM circuits, low power SRAM circuits. | |
| 6 | Low Power Microprocessor Design System: power management support, architectural trade offs for power, choosing the supply voltage, low-power clocking, implementation problem for low power, comparison of microprocessors for power & performance. | |

Reference Books:

1. P. Rashinkar, Paterson and L. Singh, "Low Power Design Methodologies", Kluwer Academic, 2002
2. Kaushik Roy, Sharat Prasad, "Low power CMOS VLSI circuit design", John Wiley sons Inc.,2000.
3. J.B.Kulo and J.H Lou, "Low voltage CMOS VLSI Circuits", Wiley, 1999.
4. A.P.Chandrasekaran and R.W.Broadersen, "Low power digital CMOS design", Kluwer,1995
5. Gary Yeap, "Practical low power digital VLSI design", Kluwer, 1998.



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Course Outcome:

After learning the course the students should be able to:

| Sr. No. | CO statement | Marks % weightage |
|---------|--|-------------------|
| CO-1 | Identify the sources of power dissipation in digital IC systems & understand the impact of power on system performance and reliability | |
| CO-2 | Characterize and model power consumption & understand the basic analysis methods. | |
| CO-3 | Understand leakage sources and reduction techniques. | |