GUJARAT TECHNOLOGICAL UNIVERSITY

Master of Engineering
Subject Code: 3726104
Semester – II
Subject Name: SoC Design

Type of course: Elective

Prerequisite: NA

Rationale:

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks				Total Marks
L	T	P	C	Theory Marks		Practical Marks		
				ESE(E)	PA (M)	PA (V)	PA (I)	
3	0	2	4	70	30	30	20	150

Content:

Sr. No.	Content	Total Hrs
1	ASIC - Overview of ASIC types, design strategies, CISC, RISC and NISC approaches for SOC architectural issues and its impact on SoC design methodologies, Application Specific Instruction Processor (ASIP) concepts.	
2	NISC - NISC Control Words methodology, NISC Applications and Advantages, Architecture Description Languages (ADL) for design and verification of Application Specific Instruction set Processors (ASIP), No-Instruction-Set-computer (NISC)- design flow, modeling NISC architectures and systems, use of Generic Netlist Representation - A formal language for specification, compilation and synthesis of embedded processors.	
3	Simulation: Different simulation modes, behavioural, functional, static timing, gate level, switch level, transistor/circuit simulation, design of verification vectors, Low power FPGA, Reconfigurable systems, SoC related modeling of data path design and control logic, Minimization of interconnects impact, clock tree design issues	
4	Low power SoC design / Digital system: Design synergy, Low power system perspective-power gating, clock gating, adaptive voltage scaling (AVS), Static voltage scaling, Dynamic clock frequency and voltage scaling (DCFS), building block optimization, building block memory, power down techniques, power consumption verification	
5	Synthesis: Role and Concept of graph theory and its relevance to synthesizable constructs, Walks, trails paths, connectivity, components, mapping/visualization, nodal and admittance graph. Technology independent and technology dependent approaches for synthesis, optimization constraints, Synthesis report analysis Single core and Multi core systems, dark silicon issues, HDL coding techniques for minimization of power consumption, Fault tolerant designs	
6	Case study for overview of cellular phone design with emphasis on area optimization, speed improvement and power minimization *Note:* Students will prepare and present a term paper on relevant identified current topics (in batches of three students per topic) as a part of theory course.	

Reference Books:

1. Hubert Kaeslin, "Digital Integrated Circuit Design: From VLSI Architectures to CMOS Fabrication", Cambridge University Press, 2008
2. B. Al Hashimi, "System on chip-Next generation electronics", The IET, 2006
3. RochitRajsuman, "System-on- a-chip: Design and test", Advantest America R & D Center, 2000
4. P Mishra and N Dutt, "Processor Description Languages", Morgan Kaufmann, 2008
5. Michael J. Flynn and Wayne Luk, "Computer System Design: System-on-Chip". Wiley, 2011

Course Outcome:

After learning the course the students should be able to:

Sr. No.	CO statement	Marks % weightage
CO-1	Identify and formulate a given problem in the framework of SoC based design approaches	
CO-2	Design SoC based system for engineering applications	
CO-3	Realize impact of SoC on electronic design philosophy and Macro-electronics thereby incline towards entrepreneurship & skill development	