GUJARAT TECHNOLOGICAL UNIVERSITY

Master of Engineering
Subject Code: 3726102
Semester – II
Subject Name: VLSI Design Verification and Testing

Type of course: Core III

Prerequisite: NA

Rationale:

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks				Total Marks
L	T	P	C	Theory Marks		Practical Marks		
				ESE(E)	PA (M)	PA (V)	PA (I)	
3	0	2	4	70	30	30	20	150

Content:

Sr. No.	Content	Total Hrs
1	Verification guidelines: Verification Process, Basic Testbench functionality, directed testing, Methodology basics, Constrained-Random stimulus, Functional coverage, Testbench components, Layered testbench, Building layered testbench, Simulation environment phases, Maximum code reuse, Testbench performance.	
2	Data types: Built-in data types, Fixed-size arrays, Dynamic arrays, Queues, Associative arrays, Linked lists, Array methods, Choosing a storage type, Creating new types with typedef ,Creating user-defined structures, Type conversion, Enumerated types, Constants strings, Expression width.	
3	Procedural statements and routines: Procedural statements, tasks, functions and void functions, Routine arguments, Returning from a routine, Local data storage, Time values Connecting the testbench and design: Separating the testbench and design, Interface constructs, Stimulus timing, Interface driving and sampling, Connecting it all together, Top-level scope Program – Module interactions.	
4	SystemVerilog Assertions: Basic OOP: Introduction, think of nouns, Not verbs, your first class, where to define a class, OOP terminology, Creating new objects, Object de-allocation, Using objects, Static variables vs. Global variables, Class methods, Defining methods outside of the class, Scoping rules, Using one class inside another, Understanding dynamic objects, Copying objects, Public vs. Local, Straying off course building a testbench	
5	Randomization: Introduction, What to randomize, Randomization in SystemVerilog, Constraint details solution probabilities, Controlling multiple constraint blocks, Valid constraints, In-line constraints, The pre_randomize and post_randomize functions,	
6	Random number functions, Constraints tips and techniques, Common randomization problems, Iterative and array constraints, Atomic stimulus generation vs. Scenario generation, Random control, Random number generators, Random device configuration.	

Reference Books:

1. Chris Spears, " System Verilog for Verification", Springer, 2nd Edition
2. M. Bushnell and V. D. Agrawal, "Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits", Kluwer Academic Publishers.
3. IEEE 1800-2009 standard (IEEE Standard for SystemVerilog— Unified Hardware Design, Specification, and Verification Language).
4. System Verilog website – www.systemverilog.org
5. http://www.sunburstdesign.com/papers/CummingsSNUG2006Boston_SystemVerilog Events.pdf
6. General reuse information and resources www.design-reuse.com
7. OVM, UVM(on top of SV) www.verificationacademy.com
8. Verification IP resources: http://www.cadence.com/products/fv/verification_ip/pages/default.aspx
9. http://www.synopsys.com/Tools/Verification/FunctionalVerification/VerificationIP/Pages/default.aspx

Course Outcome:

After learning the course the students should be able to:

Sr. No.	CO statement	Marks % weightage
CO-1	Familiarity of Front end design and verification techniques and create reusable test environments	
CO-2	Verify increasingly complex designs more efficiently and effectively.	
CO-3	Use EDA tools like Cadence, Mentor Graphics.	

List of Assignments:

1. Sparse memory
2. Semaphore
3. Mail box
4. Classes
5. Polymorphism
6. Coverage
7. Assertions