



# GUJARAT TECHNOLOGICAL UNIVERSITY

Master of Engineering

Subject Code: 3726101

Semester – II

Subject Name: Analog and Digital CMOS VLSI Design

Type of course: Core III

Prerequisite: NA

Rationale:

Teaching and Examination Scheme:

Teaching Scheme			Credits C	Examination Marks				Total Marks
L	T	P		Theory Marks		Practical Marks		
			ESE(E)	PA (M)	PA (V)	PA (I)		
3	0	2	4	70	30	30	20	150

Content:

Sr. No.	Content	Total Hrs
	Technology Scaling and Road map, Scaling issues, Standard 4 mask NMOS Fabrication process. <b>Digital CMOS Design:</b>	
1	Review: Basic MOS structure and its static behavior, Quality metrics of a digital design: Cost, Functionality, Robustness, Power, and Delay, Stick diagram and Layout, Wire delay models. Inverter: Static CMOS inverter, Switching threshold and noise margin concepts and their evaluation, Dynamic behavior, Power consumption	
2	Physical design flow: Floor planning, Placement, Routing, CTS, Power analysis and IR drop estimation-static and dynamic, ESD protection-human body model, Machine model. Combinational logic: Static CMOS design, Logic effort, Ratioed logic, Pass transistor logic, Dynamic logic, Speed and power dissipation in dynamic logic, Cascading dynamic gates, CMOS transmission gate logic	
3	Sequential logic: Static latches and registers, Bi-stability principle, MUX based latches, Static SR flip-flops, Master-slave edge-triggered register, Dynamic latches and registers, Concept of pipelining, Pulse registers, Non-bistable sequential circuit. Advanced technologies: Giga-scale dilemma, Short channel effects, High-k, Metal Gate Technology, FinFET, TFET etc <b>Analog CMOS Design:</b>	
4	Single Stage Amplifier: CS stage with resistance load, Divide connected load, Current source load, Triode load, CS stage with source degeneration, Source follower, Common gate stage, Cascade stage, Choice of device models. Differential Amplifiers: Basic difference pair, Common mode response, Differential pair with MOS loads, Gilbert cell.	
5	Passive and active current mirrors: Basic current mirrors, Cascade mirrors, Active current mirrors. Frequency response of CS stage: Source follower, Common gate stage, Cascade stage and difference pair, Noise	
6	Operational amplifiers: One stage OPAMP, Two stage OPAMP, Gain boosting, Common mode feedback, Slew rate, PSRR, Compensation of 2 stage OPAMP, Other compensation techniques.	



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## Reference Books:

1. J P Rabaey, A P Chandrakasan, B Nikolic, "Digital Integrated circuits: A design perspective", Prentice Hall electronics and VLSI series, 2nd Edition.
2. Baker, Li, Boyce, "CMOS Circuit Design, Layout, and Simulation", Wiley, 2nd Edition.
3. BehzadRazavi, "Design of Analog CMOS Integrated Circuits", TMH, 2007.
4. Phillip E. Allen and Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford, 3<sup>rd</sup> Edition.
5. R J Baker, "CMOS circuit Design, Layout and Simulation", IEEE Inc., 2008.
6. Kang, S. and Leblebici, Y., "CMOS Digital Integrated Circuits, Analysis and Design", TMH, 3rdEdition.
7. Pucknell, D.A. and Eshraghian, K., "Basic VLSI Design", PHI, 3rd Edition.

## Course Outcome:

After learning the course the students should be able to:

Sr. No.	CO statement	Marks % weightage
CO-1	Analyze, design, optimize and simulate analog and digital circuits using CMOS constrained by the design metrics	
CO-2	Connect the individual gates to form the building blocks of a system	
CO-3	Use EDA tools like Cadence, Mentor Graphics and other open source software tools like Ngspice	
CO-4	Design digital and analog Circuit using CMOS	

## List of Experiments:

- 1) Use VDD=1.8V for 0.18um CMOS process, VDD=1.3V for 0.13um CMOS Process and VDD=1V for 0.09um CMOS Process.
  - a) Plot ID vs. VGS at different drain voltages for NMOS, PMOS.
  - b) Plot ID vs. VGS at particular drain voltage (low) for NMOS, PMOS and determine Vt.
  - c) Plot log ID vs. VGS at particular gate voltage (high) for NMOS, PMOS and determine IOFF and sub threshold slope.
  - d) Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
  - e) Extract Vth of NMOS/PMOS transistors (short channel and long channel). Use VDS = 30mV  
To extract Vth use the following procedure.
    - i. Plot gm vs VGS using NGSPICE and obtain peak gm point.
    - ii. Plot  $y=ID/(gm)^{1/2}$  as a function of VGS using Ngspice.
    - iii. Use Ngspice to plot tangent line passing through peak gm point in y (VGS) plane and determine Vth.
  - f) Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency.Tabulate your result according to technologies and comment on it.



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- 2) Use  $V_{DD}=1.8V$  for 0.18 $\mu m$  CMOS process,  $V_{DD}=1.2V$  for 0.13 $\mu m$  CMOS Process and  $V_{DD}=1V$  for 0.09 $\mu m$  CMOS Process.
  - a) Perform the following
    - i. Plot VTC curve for CMOS inverter and thereon plot  $dV_{out}$  vs.  $dV_{in}$  and determine transition voltage and gain g. Calculate  $V_{IL}$ ,  $V_{IH}$ ,  $N_{MH}$ ,  $N_{ML}$  for the inverter.
    - ii. Plot VTC for CMOS inverter with varying  $V_{DD}$ .
    - iii. Plot VTC for CMOS inverter with varying device ratio.
  - b) Perform transient analysis of CMOS inverter with no load and with load and determine  $t_{pHL}$ ,  $t_{pLH}$ , 20%-to-80%  $t_r$  and 80%-to-20%  $t_f$ . (use  $V_{PULSE} = 2V$ ,  $C_{load} = 50fF$ )
  - c) Perform AC analysis of CMOS inverter with fanout 0 and fanout 1. (Use  $C_{in} = 0.012pF$ ,  $C_{load} = 4pF$ ,  $R_{load} = k$ )
  
- 3) Use Ngspice to build a three stage and five stage ring oscillator circuit in 0.18 $\mu m$  and 0.13 $\mu m$  technology and compare its frequencies and time period.
  
- 4) Perform the following
  - a) Draw small signal voltage gain of the minimum-size inverter in 0.18 $\mu m$  and 0.13 $\mu m$  technology as a function of input DC voltage. Determine the small signal voltage gain at the switching point using Ngspice and compare the values for 0.18 $\mu m$  and 0.13 $\mu m$  process.
  - b) Consider a simple CS amplifier with active load, as explained in the lecture, with NMOS transistor MN as driver and PMOS transistor MP as load, in 0.18 $\mu m$  technology.  $(W/L)_{MN}=5$ ,  $(W/L)_{MP}=10$  and  $L=0.5\mu m$  for both transistors.
    - i. Establish a test bench, as explained in the lecture, to achieve  $V_{DSQ}=V_{DD}/2$ .
    - ii. Calculate input bias voltage if bias current= $50\mu A$ .
    - iii. Use Ngspice and obtain the bias current. Compare its value with  $50\mu A$ .
    - iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier using small signal analysis in Ngspice (consider 30fF load capacitance).
    - v. Plot step response of the amplifier for input pulse amplitude of 0.1V. Derive time constant of the output and compare it with the time constant resulted from -3dB BW
    - vi. Use Ngspice to determine input voltage range of the amplifier
  
- 5) Three OPAMP INA.  $V_{dd}=1.8V$   $V_{ss}=0V$ , CAD tool: Mentor Graphics DA. Note: Adjust accuracy options of the simulator (setup->options in GUI). Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.
  - i. Draw the schematic of op-amp macro model.
  - ii. Draw the schematic of INA.
  - iii. Obtain parameters of the op-amp macro model such that
    - a. low-frequency voltage gain =  $5 \times 10^4$ ,
    - b. unity gain BW ( $f_u$ ) = 500KHz,
    - c. input capacitance= $0.2pF$ ,
    - d. output resistance =  $\infty$ ,
    - e. CMRR= $120dB$
  - iv. Draw schematic diagram of CMRR simulation setup.
  - v. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).
  - vi. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches.
  - vii. Repeat (iii) to (vi) by considering CMRR of all OPAMPs to be 90dB.



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- 6) Technology: UMC 0.18 $\mu$ m, VDD=1.8V. Use MAGIC or Microwind.
- Draw layout of a minimum size inverter in UMC 0.18 $\mu$ m technology using MAGIC Station layout editor. Use that inverter as a cell and lay out three cascaded minimum-sized inverters. Use M1 as interconnect line between inverters.
  - Run DRC, LVS and RC extraction. Make sure there is no DRC error. Extract the netlist.
  - Use extracted netlist and obtain tPHLtPLH for the middle inverter using Eldo.
  - Use interconnect length obtained and connect the second and third inverter.

Extract the new netlist and obtain tPHL and tPLH of the middle inverter. Compare new values of delay times with corresponding values obtained in part 'c'.