GUJARAT TECHNOLOGICAL UNIVERSITY

Subject Name: System on Chip Architecture(Elective)
Subject Code: 3725205
Semester II

Type of course: ME-Electronics & Communication Engineering (VLSI & Embedded Systems Design**)**

Prerequisite: Network on chip

Rationale: NA

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks				Total Marks
L	T	P	C	Theory Marks		Practical Marks		
				ESE (E)	PA (M)	ESE(V)	PA (I)	
4	2#	0	5	70	30	30	20	150

L- Lectures; T- Tutorial/Teacher Guided Student Activity; P- Practical; C- Credit; ESE- End Semester Examination; PA- Progressive Assessment;

Content:

Sr. No.	Content	Total Hrs	% Weightage
1	**SoC methodology** Abstract system modeling – Introduction to Transaction Level Modeling(TLM), SystemC, High Level Synthesis (HLS), specification, Requirement analysis related to power, performance and cost – Algorithms, architecture, implementation constraints; control and data path analysis, partitioning; interfacing requirements; Integration and Verification, Regression testing	6	10
	Part – I System on FPGA		
2	Embedded hard and soft processor cores in FPGAs from Altera, Xilinx and others; Interfacing processor core with user FPGA logic, IP cores and interface to processor bus, Booting methods, configuration and parametric customization, debugging, design environment, base system builder, hardware simulation flow, supported OS and porting effort, Processor bus bridging to support reusable IPs/peripherals, Case study- AXI4 bus specification; Memory organization – Internal and external memory controller design, cross- compilers for HLL programming, provision for custom instructions, Auxiliary processing units	6	20
3	Xilinx Zynq family overview, system development methodology, use of the ARM processor features like Neon, MMU, floating point unit, exception handling; Developing AXI4 based peripheral using FPGA fabric	6	10
	Part – II System on Chip		
4	Requirement analysis, Classification of SoC, Comparative study of different SoC platforms from TI, freescale, cavium, Tilera, intel, nvidia, Qualcomm, Cypress, netronome, ezchip and more etc…- Key features, accelerator engines, application domains like graphics, DSP, image processing, audio-video encoding-decoding, security, encryption-decryption, Power efficiency, performance criteria	6	10

5	Cypress PSoC family; Overview, system development methodology, Analog mixed signal design flow; Case studies – Analog sensing, DSP, memory access, networking, PWM; hardware-software co-design	7	20

Reference Books:

1. Zynq data sheets www.xilinx.com
2. PSoC documentation www.cypress.com/psoc

Course Outcome:

After learning the course the students should be able to:

1. Understand about the modelling and synthesis in SOC methodology.
2. Analyse about the working of FPGAs from Altera, Xilinx.
3. Evaluate the development methodology use of the ARM processor and its features.
4. Understand about the different SOC platforms from Intel, Intel, NVidia, ezchip etc.
5. Analyse the analog mixed signal design flow with networking

List of Experiments: (with Open Ended Problems)

1. Design a SOC to interface 8 bit LED to the ZYNQ processor.

List of Open Source Software/learning website:

1. **Xilinx ISE vivado webpack.**

Review Presentation (RP): The concerned faculty member shall provide the list of peer reviewed Journals and Tier-I and Tier-II Conferences relating to the subject (or relating to the area of thesis for seminar) to the students in the beginning of the semester. The same list will be uploaded on GTU website during the first two weeks of the start of the semester. Every student or a group of students shall critically study 2 papers, integrate the details and make presentation in the last two weeks of the semester. The GTU marks entry portal will allow entry of marks only after uploading of the best 3 presentations. A unique id number will be generated only after uploading the presentations. Thereafter the entry of marks will be allowed. The best 3 presentations of each college will be uploaded on GTU website