GUJARAT TECHNOLOGICAL UNIVERSITY

Subject Name: Designing with Modeling & FPGA's (Elective)
Subject Code: 3725204

Semester II

Type of course: ME - Electronics & Communication Engineering (VLSI & Embedded Systems Design

Prerequisite: Digital CMOS VLSI Design

Rationale: NA

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks				Total Marks
L	T	P	C	Theory Marks		Practical Marks		
				ESE (E)	PA (M)	ESE(V)	PA (I)	
4	2#	0	5	70	30	30	20	150

L- Lectures; T- Tutorial/Teacher Guided Student Activity; P- Practical; C- Credit; ESE- End Semester Examination; PA- Progressive Assessment;

Content:

Sr. No.	Content	Total Hrs	% Weightage
1	**Review of transistor operation, Single stage amplifiers, Differential amplifier** MOS I/V characteristics. Transistor second order effects. Small signal analysis. Small signal model. Gain of common-source stage amplifier using small signal analysis. Common-source stage with resistive load, diode-connected load, current-source load, triode load, source degeneration. Source follower stage. Common-gate stage. Cascade stages. Single-ended and differential operation. Basic differential pair. Common-mode response. Differential pair with MOS loads. Gilbert Cell	6	10
2	**Current Mirrors, Response of Amplifiers, Noise characteristics** Basic and cascade current mirrors. Using active current mirrors as loads. The Miller theorem. Frequency response of source follower, common-gate amplifier, cascade stage, differential pair. Noise characteristics. Noise types: thermal noise, flicker noise. Representation of noise in circuits. Properties of feedback circuits. Feedback Configurations. Effect of loading in feedback	6	20
3	**Operational amplifiers** Operational amplifier's performance parameters. One-Stage Op Amps. Two-Stage Op Amp. Op Amps Gain Boosting. Op Amps Common-Mode Feedback. Op Amps Input Range Limitation: unity-gain buffer, extension of input CM range, variation of equivalent transconductance with the input CM level. Op Amps Slew Rate. Noise in Op Amps and Power Supply Rejection.Stability and Frequency compensation	6	10
4	**Bandgap References, Switched-capacitor circuits, Nonlinearity** Supply-independent biasing. Temperature- independent references: negative-TC voltage, positive-TC voltage, bandgap reference. PTAT current generation. Speed and noise issues. Continuous-time feedback amplifier using	6	10

	resistors, capacitors, switched-capacitor amplifier in sampling mode, amplification mode, transfer of capacitor's charges. Sampling switches. Switched-capacitor amplifiers. Switched-capacitor integrator. Nonlinearity. Mismatch. Ring oscillators. LC oscillators. Voltage-controlled oscillators. Mathematical models of VCOs		
5	**Phase-locked loops, Data converters, charge-coupled devices (CCD)** Simple PLL. Charge-pump PLLs. Non ideal effects in PLLs: PFD/CP non idealities, jitter in PLLs. Delay- locked loops. PLL applications. Analog versus discrete time signals. Sample and hold characteristics .ADC and DAC specifications. DAC architectures. ADC architectures. Sampling and aliasing, Quantization noise & Data Converter SNR. CCD imaging and architecture	6	20

Reference Books:

1. R.J. Baker, H.W. Li, D.E. Boyce. CMOS. Circuit design, Layout, and Simulation (2nd Edition), 2005.
2. P. Horowitz, W. Hill, Electronic Circuit Design: Art and Practice, 2001. 192p.
3. B. Razavi, Design of Analog CMOS Integrated Circuits, 2000. 684p.
4. R.J. Baker, CMOS Mixed-Signal Circuit Design, 2002. 502p
5. B. Razavi. Principles of Data Conversion System Design. 1994

Course Outcome:

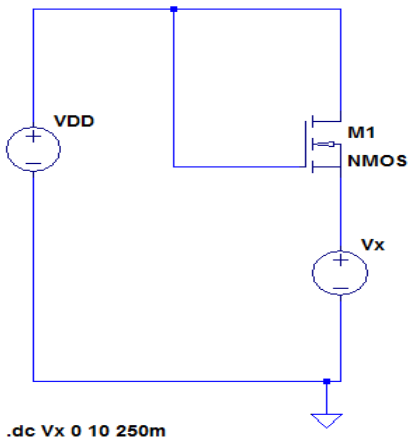
1. After learning the course the students should be able to:
2. Analyse about the transistor operations and single stage amplifiers.
3. Understand the basic about working of current mirrors and response of amplifiers.
4. Evaluate about the different modes in operational amplifiers with their characteristics.
5. Analyse the speed and noise issues in switched capacitors circuits and study about nonlinearity.
6. Understand about the working of phase locked loop and its applications and data converters.

List of Experiments: (with Open Ended Problems)

1. For W/L=50/0.5,plot the drain current of an NMOS and a PMOS as a function of VGS as VDS varies from 0 to 3v.assume VDS=3v.

2. Plot the output characteristics of NMOS and PMOS,(Id vs Vds). Identify the variations in output current, when channel length is reduced.
3. Sketch Ix vs Vx for the following circuit and write your observation.

   a)



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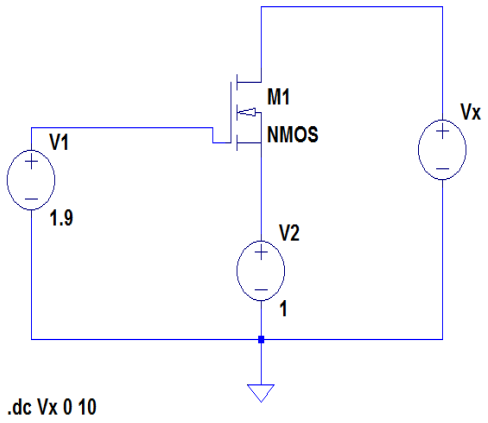
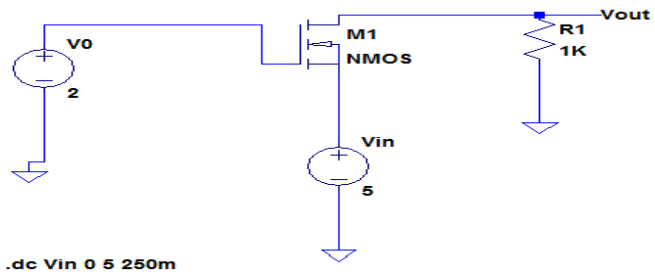
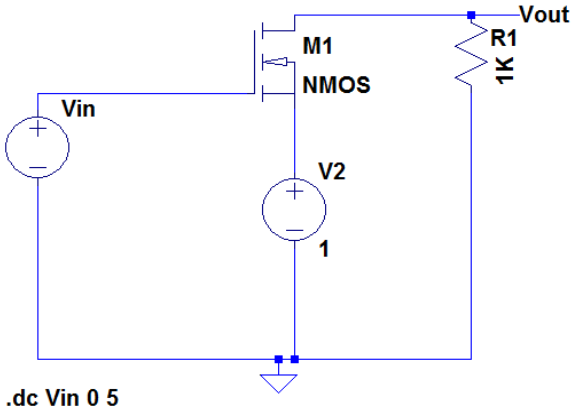


4. Sketch Vout as a function of Vin for the following.

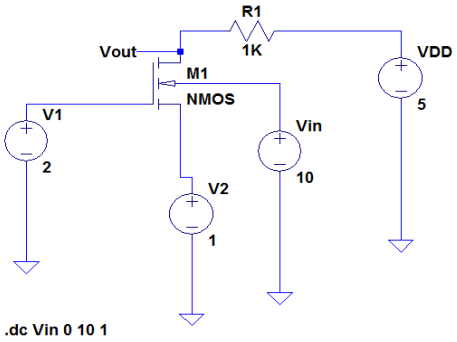
a)



b)

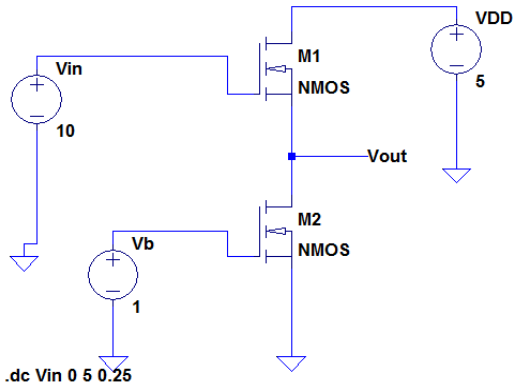


5. Sketch Vout as a function of Vin for the following.

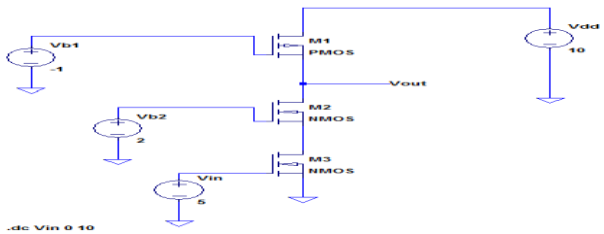


6. Sketch Vout as a Vin for the following circuit(Vin varies from o to VDD).

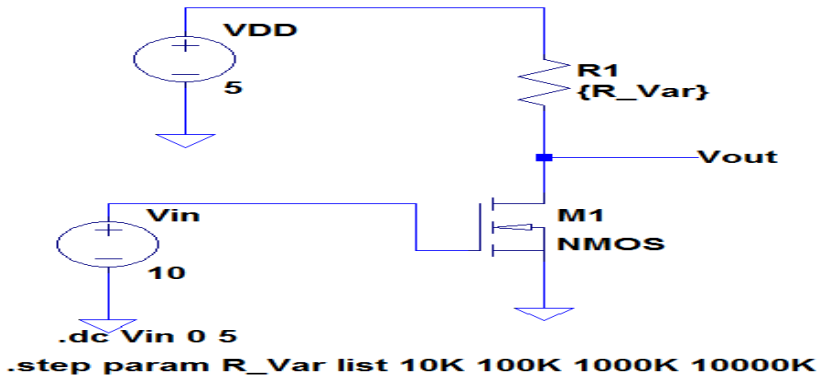
a)



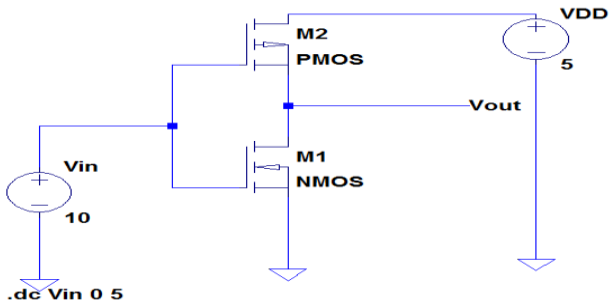
b)



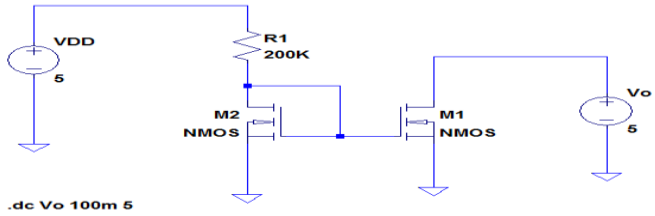
c) R varies from 10k to 10M



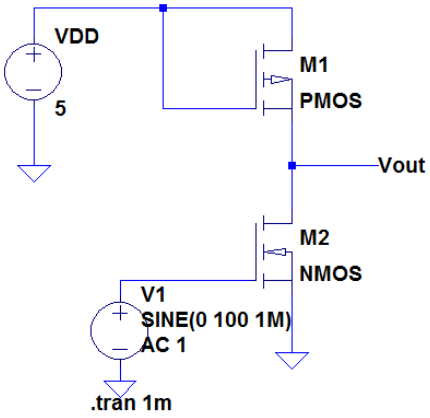
7. Plot the cmos inverter transfer characteristics(vout vs vin).



8. Plot vout vs Id(M1) and I2(M2) for the following

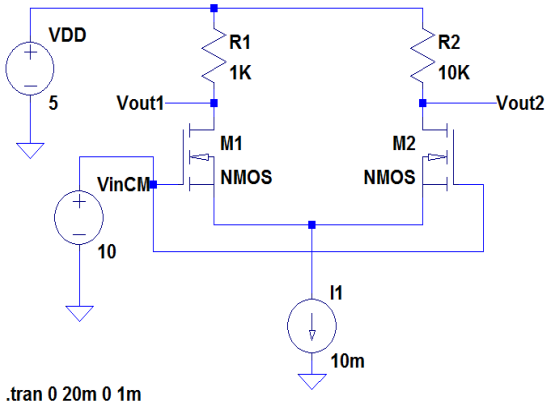


9. Plot transient analysis, showing amplification done by common source amplifier.

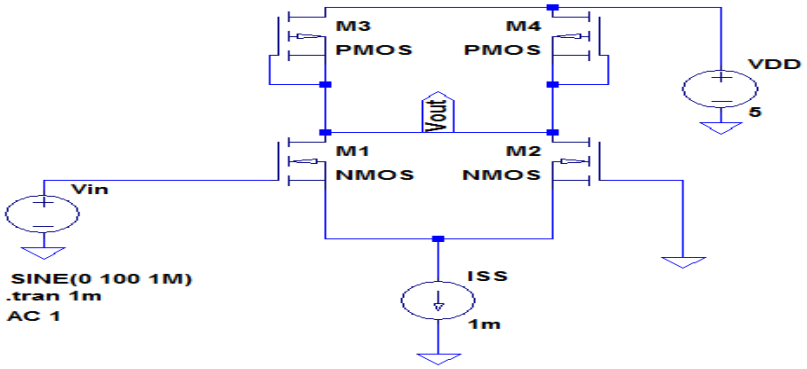


10. Plot common mode response of a differential amplifier.

a)



b)



Major Equipment's:

List of Open Source Software/learning website:

1. **LT Spice**

Review Presentation (RP): The concerned faculty member shall provide the list of peer reviewed Journals and Tier-I and Tier-II Conferences relating to the subject (or relating to the area of thesis for seminar) to the students in the beginning of the semester. The same list will be uploaded on GTU website during the first two weeks of the start of the semester. Every student or a group of students shall critically study 2 papers, integrate the details and make presentation in the last two weeks of the semester. The GTU marks entry portal will allow entry of marks only after uploading of the best 3 presentations. A unique id number will be generated only after uploading the presentations. Thereafter the entry of marks will be allowed. The best 3 presentations of each college will be uploaded on GTU website