GUJARAT TECHNOLOGICAL UNIVERSITY

Subject Name: Digital VLSI Design – II Backend
Subject Code: 3725203

Semester II

Type of course: ME - Electronics & Communication Engineering (VLSI & Embedded Systems Design

Prerequisite: Digital VLSI System Design

Rationale: NA

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks				Total Marks
L	T	P	C	Theory Marks		Practical Marks		
				ESE (E)	PA (M)	ESE(V)	PA (I)	
4	2#	0	5	70	30	30	20	150

L- Lectures; T- Tutorial/Teacher Guided Student Activity; P- Practical; C- Credit; ESE- End Semester Examination; PA- Progressive Assessment;

Content:

Sr. No.	Content	Total Hrs	% Weightage
1	**Recap of Front-end flow and Logic Synthesis.** Recap Units II and IV of Course Digital VLSI Design I – Front-end	6	10
2	**Physical Design Setup and Floor planning** VLSI Design Cycle, Methodology of Physical Design, Simplified Cycle of Physical IC Design, Partitioning, Floor planning, Placement, Routing, Compaction, Verification. Logical libraries, Physical Libraries, Timing Constraints, Database format, Logical data setup, Physical data setup, Technology Files, Interconnect delay models, tcl scripting for automation. Hierarchical Design Planning Flow, Pad Creation and Order Assignments, Core Area, Initializing the Floorplan, Timing Driven Placement, Placement with Hierarchical Gravity, Analyze placement and Color Modules, Post-initialization Macro placement controls, Large Macro Handling, Power Network Synthesis (PNS), Power Network Analysis (PNA)	6	10
3	**Placement** Placement Methodology, Fast Iteration with Coarse Placement, Understanding the Congestion Calculation, Textual Congestion Report, Analyzing the Congestion Map, Global Route (GR) for Congestion Map, Strategies for Fixing Congestion Problems, Congestion-Driven Placement Options, Adjusting Cell Density, Timing and Power Optimization for Best QoR, Congestion-Driven Placement, Incremental Congestion Refinement, Refinement Flow, Incremental mode, Area Recovery, Timing Analysis	7	10
4	**Clock Tree Synthesis** Design Status, Start of CTS Phase, Clock Tree Synthesis, CTS Goals, Define Clock Root Attributes, Stop, Float and Exclude Pins, Generated and Gated Clocks , User-defined or Explicit Stop Pins, Defining an Explicit Float Pin, Preserving Pre-Existing Clock Trees, Impact of Preexisting Clock Cells,	7	20

	Logical Design Rule Constraints, Non-Default Clock Routing, Specifying Non-Default Rules, Non-default Rule Options, Effects of Clock Tree Synthesis, Incremental Placement / Optimization, Analysis using the CTS GUI , Clock Tree Optimization, Inter-Clock Delay Balancing, Post Route CTO		
5	**Routing and Post Tapeout flow** Design Status, Start of Routing Phase, Grid-Based Routing System, Routing over Macros, Pre-Route Checks, Routing Operations, Core Routing Strategy, Fixing DRC Violations, Crosstalk-Induced Noise, Crosstalk-Induced Delay, Crosstalk Prevention, Crosstalk Correction, Wire Sizing.	7	20

Reference Books:

1. J.P. Uyenmura. Introduction to VLSI Circuits and Systems, J.Wiley & Sons, 2002.
2. J.M. Rabaey, A. Chandrakasan, B. Nikolic. Digital Integrated Circuits – A Design Perspective, Prentice Hall, 2003.
3. J.P. Uyenmura. Modern VLSI Design - System-on-Chip Design, Prentice-Hall, 2002.

Course Outcome:

1. After learning the course the students should be able to:
2. Understand the physical design flow in VLSI including floor planning and routing.
3. Analyse the physical design and automation of FPGs & MCMS.
4. Analyse the different way of placement in the VLSI Design flow.
5. Analyse about the clock tree synthesis and its goals.
6. Evaluate the different ways of routing and study about DRC violations and cross talk correction.

List of Experiments: (with Open Ended Problems)

1. What are inputs of physical design and what does each of input contain?
2. What is importance of Floor plan? Once Floor-plan is completed what are all check you will be ensure??? Explain in detail process of Floor-plan?
3. What is importance of Placement? Once Placement is done what are all checks you will be ensure??? Explain in detail process of Placement?
4. What is importance of CTS? Once CTS is Completed what are all checks you will be ensure?? Explain I detail process of CTS?
5. Define Insertion Delay, Input delay, Output Delay, Global Skew, Effective Skew, Source Latency, Network Latency?
6. Explain in Detail Min Pulse width Setup, Hold, Recovery and Removal Checks?
7. What is importance of Routing? Once Routing is done what are all checks you will be ensure?? Explain in detail process of routing?
8. What is Antenna Violation and ways to prevent it?
9. What is EM Violation and ways to prevent it?
10. What are Different Congestion techniques involved explain each of them in detail?
11. What are Different timing paths explain? And what are different timing exceptions explain?

Major Equipments:

List of Open Source Software/learning website:

1. **IC compiler, Mentor Graphics**

Review Presentation (RP): The concerned faculty member shall provide the list of peer reviewed Journals and Tier-I and Tier-II Conferences relating to the subject (or relating to the area of thesis for seminar) to the students in the beginning of the semester. The same list will be uploaded on GTU website during the first two weeks of the start of the semester. Every student or a group of students shall critically study 2 papers, integrate the details and make presentation in the last two weeks of the semester. The GTU marks entry portal will allow entry of marks only after uploading of the best 3 presentations. A unique id number will be generated only after uploading the presentations. Thereafter the entry of marks will be allowed. The best 3 presentations of each college will be uploaded on GTU website