GUJARAT TECHNOLOGICAL UNIVERSITY

Master of Engineering
Subject Code: 3722613
Semester – II
Subject Name: Mixed Signal CMOS Circuits

Type of course: Advanced MOSFET based analog circuit design

Prerequisite: MOSFET modeling and basic CMOS circuit design

Rationale: This course provides a platform for students to apply basic knowledge of working of MOSFETs to analyze and design complex analog and mixed signal circuits such as phased locked loops, bandgap references, analog to digital converters and digital to analog converters, memory circuits, switched capacitor circuits, and comparator circuits, etc.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks				Total Marks
				Theory Marks		Practical Marks		
L	T	P	C	ESE (E)	PA (M)	ESE (V)	PA (I)	
3	0	2	4	70	30	30	20	150

Content:

Sr. No.	Content	Total Hrs
1	**Bandgap References:** General Considerations, Supply-Independent Biasing, Temperature Independent References, PTAT Current Generation, Constant Gm Biasing, Speed and Noise Issues, Case Study	7
2	**Memory Circuits:** Introduction, Sensing Basics, Folded Array, Chip Organization, Sense Amplifier Design, Row/Column Decoder, Row Drivers, SRAM Cell, ROM, Floating Gate Memory, Sensing using Modulation: Examples of DSM, Using DSM for sensing in Flash Memory, Sensing Resistive Memory, Sensing in CMOS Images	8
3	**Phase-Locked Loops:** Simple PLL, Charge-Pump PLLs, Non ideal Effects in PLLs, Delay Locked Loops, Applications	9
4	**Digital-Analog and Analog-Digital Converters:** Introduction and Characterization of DAC, Parallel DAC, Introduction and Characterization of ADC, Serial ADC	6
5	**Introduction to Switched-Capacitor Circuits:** General Considerations, Sampling switches, Switched-Capacitor Amplifiers, Switched-Capacitor Integrator, Switched-Capacitor Common-Mode Feedback	8
6	**Nonlinear Analog Circuits:** Basic CMOS Comparator Design, Characterizing the Comparator, Clocked Comparators, Adaptive Biasing, Analog Multipliers	4

Suggested Specification table with Marks (Theory):

Distribution of Theory Marks					
R Level	U Level	A Level	N Level	E Level	C Level
20	**30**	**20**	**10**	**10**	**10**

Legends: R: Remembrance; U: Understanding; A: Application, N: Analyze and E: Evaluate C: Create and above Levels (Revised Bloom's Taxonomy)

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Reference Books:

1. Design of Analog CMOS Integrated Circuits, Behzad Razavi, TMH
2. CMOS Circuit Design, Layout, and Simulation, R. Jacob Baker, Wiley, 2nd Edition
3. RF Microelectronics, Behzad Razavi, Pearson, 2nd Edition

Course Outcomes:

Sr. No.	CO statement	Marks % weightage
CO-1	Analyze and design bandgap reference circuit.	20 %
CO-2	Analyze and design various blocks of memories.	20 %
CO-3	Analyze basic and charge pump PLL as well as related design issues.	20 %
CO-4	Analyze DAC and ADC, and its design issues.	10 %
CO-5	Analyze switched capacitor circuits as well as related design issues.	20 %
CO-6	Analyze CMOS comparator circuits as well as related design issues.	10 %

List of Experiments:

Perform experiments 1 to 11 in 180 nm technology.

1. To simulate self-biased supply independent band-gap reference circuit with and without startup circuit, and obtain its current response as a function of variation in supply voltage.

2. To verify through simulation that NMOS is poor conductor of '1', PMOS is poor conductor of '0,' and transmission gate is good conductor of '1' and '0'.
3. To obtain ON resistance of following devices when used a switch using simulation: 1. NMOS 2. PMOS 3. Transmission Gate .
4. To obtain the error in sampled voltage when following devices used a switch using simulation: 1. NMOS 2. PMOS 3. Transmission Gate.
5. To study and simulate dummy device based charge injection cancellation technique. Obtain the error in sampled voltage.
6. To simulate switched capacitor amplifier circuit.
7. To simulate basic clock signal based sense amplifier circuit and measure its performance parameters.
8. To simulate and analyze charge pump PLL.
9. To simulate regenerative feedback based CMOS comparator circuit and measure its performance parameters.
10. To simulate 1-bit DRAM and measure its performance parameters.
11. To simulate 1-bit SRAM and measure its performance parameters.
12. Perform above experiments in 90 nm technology also and compare as well give comments on your results.
13. Seminar report for a given research topic.

Major Equipment:

C.R.O., Function Generator, Power Supply, Multimeter, Digital Storage Oscilloscope.

List of Open Source Software/learning website:

1. ngspice/multisim (software)
2. www.nptel.ac.in
3. www.ocw.mit.edu
4. www.mosis.com
5. www.berkeley.edu