GUJARAT TECHNOLOGICAL UNIVERSITY

Master of Engineering
Subject Code: 3722612

Semester – II
Subject Name: VLSI Signal Processing Systems

Type of course: Basic subject on methodologies to design VLSI system for signal processing applications

Prerequisite: Knowledge of basic CMOS circuit design

Rationale: The field of signal processing has always been driven by the advances in DSP applications and VLSI technologies. Therefore, at any given time, DSP applications impose several challenges on the implementations of the DSP systems. This course addresses the methodologies needed to design custom or semi-custom VLSI circuits for these applications.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks				Total Marks
L	T	P	C	Theory Marks		Practical Marks		
				ESE (E)	PA (M)	ESE (V)	PA (I)	
3	0	2	4	70	30	30	20	150

Content:

Sr. No.	Content	Total Hrs
1	**Introduction to DSP algorithms, Iteration bound:** Typical DSP algorithms: Convolution, Correlation, Digital-filters, adaptive filters etc. Data-flow graph representations, iteration bound and its computation, iteration bound of Multirate data-flow graphs.	10
2	**Pipelining, Parallel Processing and Retiming:** Pipelining of FIR filters, Parallel processing, Pipelining and Parallel Processing for low power, definitions and properties of retiming, system inequalities and its solution, retiming techniques.	8
3	**Unfolding and Folding:** Algorithm for unfolding, properties of unfolding, Comparative analysis of (i) critical path (ii) unfolding and (iii) retiming. Folding transformation, Register minimization techniques, folding of Multirate systems.	8
4	**Systolic Architecture Design:** Systolic array design methodology, FIR systolic arrays, Selection of scheduling vector, Matrix-matrix multiplication and 2D systolic array design, systolic design for space representations containing delays.	6
5	**Bit-Level Arithmetic Architecture and Redundant Arithmetic:** Parallel multipliers, Interleaved floor-plan and bit-plan based filters, Bit-serial multipliers,	10

	Bit-serial filter design and implementation, Canonic signed digit arithmetic, distributed arithmetic, Redundant number representations, Carry-free radix-2 addition and subtraction, Hybrid radix-4 addition, Hybrid redundant multiplication architectures, Data format converter.	

Suggested Specification table with Marks (Theory):

Distribution of Theory Marks					
R Level	U Level	A Level	N Level	E Level	C Level
20	**30**	**20**	**10**	**10**	**10**

Legends: R: Remembrance; U: Understanding; A: Application, N: Analyze and E: Evaluate C: Create and above Levels (Revised Bloom's Taxonomy)

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Reference Books:

1. Keshab K. Parhi, "VLSI Digital Signal Processing Systems", Wiley, 2010.
2. Magdy A. Bayoumi, E. Swartzlander, "VLSI Signal Processing Technology", Springer Science, 1994.
3. Peter B. Denyer, David Renshaw, "VLSI signal processing: a bit-serial approach", Addison-Wesley, 1985.

Course Outcomes:

Sr. No.	CO statement	Marks % weightage
CO-1	Understand the concept and requirements of iteration bound	20 %
CO-2	Apply basics of pipelining and parallel processing to design the system for high speed and low power requirements.	20 %
CO-3	Perform folding, unfolding and retiming operations on the given systems	30 %
CO-4	Implement various algorithms based on systolic architectures.	10 %
CO-5	Evaluate bit level arithmetic and redundant arithmetic techniques.	20 %

GUJARAT TECHNOLOGICAL UNIVERSITY

Master of Engineering
Subject Code: 3722612

List of Experiments:

1. Compute the iteration bound for the given data flow graph (DFG).
2. Determine the iteration bound for the given multi rate DFG.
3. For given DFG place pipelining register at appropriate places to achieve required sample rate.
4. For given DFG calculate critical path and place pipelining latches to reduce critical paths.
5. For given DFG place pipeline structure to reduce power consumption.
6. Design a given FIR filter with pipeline and parallel processing for power reduction and sampling rate improvement.
7. For given DFG apply retiming techniques to minimize the clock period.
8. Solve the problem of critical path using unfolding techniques for given DFG.
9. Design the folded architecture for the 6-tap FIR filter.
10. Design systolic-architecture for matrix-vector multiplication.
11. Design bit-parallel architecture for six-bit addition.
12. Design a MSD-first radix-4 maximally redundant to non-redundant converter for word length of 8 digits.

List of Open Source Software/learning website:

1. www.nptel.ac.in
2. www.ocw.mit.edu