



GUJARAT TECHNOLOGICAL UNIVERSITY

Master of Engineering

Subject Code: 2722606

Semester – II

Subject Name: ALGORITHMS FOR VLSI PHYSICAL DESIGN AUTOMATION

Type of course: Physical Algorithm Based Course

Prerequisite: Basic knowledge of VLSI Chip Design and Graph Theory

Rationale: This course provides a platform for students to apply basic knowledge of algorithm to understand and implement complex physical design algorithms such as Circuit Partitioning, Floor planning, Placement, Grid and Global routing etc. This course gives insight into designing of various CAD Tools.

Teaching and Examination Scheme:

Teaching Scheme			Credits C	Examination Marks				Total Marks
L	T	P		Theory Marks		Practical Marks		
				ESE (E)	PA (M)	ESE (V)	PA (I)	
3	0	2	4	70	30	30	20	150

Content:

Sr. No.	Content	Total Hrs
1	Introduction: VLSI Design Process, Layout Styles, Difficulties in Physical Design, Definitions and Notation	5
2	Circuit Partitioning: Introduction, Problem Definition, Cost Function and Constraints, Approaches to Partitioning Problem, Other Approaches and Recent Work.	5
3	Floor planning: Introduction, Problem Definition, Approaches to Floor planning, Other Approaches and Recent Work.	5
4	Placement: Introduction, Problem Definition, Cost Functions and Constraints, Approaches to Placement, Other Approaches and Recent Work.	5
5	Grid Routing: Introduction, Problem Definition, Cost Functions and Constraints, Maze Routing Algorithms, Line Search Algorithms, Other Issues, Other Approaches and Recent Work.	5
6	Global Routing: Introduction, Cost Functions and Constraints, Routing Regions, Sequential Global Routing, Integer Programming, Global Routing by Simulated Annealing, Hierarchical Global Routing, Other Approaches and Recent Work.	5
7	Channel Routing: Introduction, Problem Definition, Cost Functions and Constraints,	5



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	Approaches to Channel Routing, Other Approaches and Recent Work.	
8	Layout Generation: Introduction, Layout Generation, Standard-cell Generation, Optimization of Gate-matrix Layout, Programmable Logic Arrays, Other Approaches and Recent Work.	7

Suggested Specification table with Marks (Theory): (For BE only)

Distribution of Theory Marks (percentage)					
R Level	U Level	A Level	N Level	E Level	C Level
20	30	20	10	10	10

Legends: R: Remembrance; U: Understanding; A: Application, N: Analyze and E: Evaluate C: Create and above Levels (Revised Bloom's Taxonomy)

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Reference Books:

1. VLSI Physical Design Automation, Theory and Practice, Sadiq M. Sait and Habib Youssef. By world scientific press.
2. Algorithm for VLSI physical design automation by Sherwani and navneet- by Springer /B S Publication (2008).
3. N. Sherwani, Algorithms for VLSI Physical Automation, Third Edition, Kluwer, 1998.
4. S. H. Gerez, Algorithms for VLSI Design Automation, Wiley, 1998.
5. A. Micozo, Digital Logic Testing and Simulation, Second edition, Wiley, 2003.
6. S. M. Sait and H. Yousuf, Iterative Computer Algorithm with Applications in Engineering, Wiley/IEEE, 2002.
7. C. Visweswariah and S. Duvall, Computer Aided Optimization of Digital Integrated Circuits, Wiley, 2002.
8. G. De Micheli, Synthesis and Optimization of Digital Circuits, Mcgraw-Hill International, 1994.

Course Outcomes:

Sr. No.	CO statement	Marks % weightage
CO-1	Understand the concept of circuit partitioning and minimize the number of net crossing.	20



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CO-2	Determine the aspect ratio of each module to reduce the overall chip area.	20
CO-3	Apply different algorithms to place the circuit components on layout surface to reduce the size of chip.	20
CO-4	Understand different routing algorithms to minimize the overall wire length.	20
CO-5	Learn the generation of optimize layout for different architectures.	20

List of Experiments:

Perform experiments in either Scilab or Matlab.

- 1 Introduction to Various CAD Design Tools and its comparisons.
- 2 Implementation of Dijkstra's routing algorithm.
- 3 Implementation of the Kernighan Lin Algorithm for circuit partitioning.
- 4 Implementation of the Fiduccia Mattheyses Algorithm for circuit partitioning.
- 5 Implementation of the Simulated Annealing Algorithm.
- 6 Implementation of the Genetic Algorithm.
- 7 Implementation of Yoshimura and Kuh algorithm.
- 8 Implementation of the Linear Ordering Cluster Growth Algorithm.
- 9 Implementation of the Unconstrained Algorithm for channel routing.
- 10 Implementation of the vertical constrained Algorithm for channel routing.
- 11 Seminar report for a given research topic.
- 12 Case study: Modification in any existing algorithm.

Major Equipment: SciLAB / MATLAB

List of Open Source Software/learning website:

1. <http://wwwhome.ewi.utwente.nl/~gerezsh/cadvlsi/book.html>
2. <http://www.personal.kent.edu/~rmuhamma/GraphTheory/graphTheory.htm>
3. <http://compprog.wordpress.com/2007/11/09/minimal-spanning-trees-prim-algorithm/>
4. <http://www.people.vcu.edu/~gasmerom/MAT131/mst.html>
5. <http://www.personal.kent.edu/~rmuhamma/GraphTheory/MyGraphTheory/trees.htm>
6. <http://graphics.stanford.edu/courses/cs448b-02-winter/lectures/treesgraphs/tree.graph.pdf>
7. <http://www.slideshare.net/purpleinkredshirt/introduction-to-graph-theory>
8. <http://lecturesppt.blogspot.in/2011/09/graphs-and-algorithms-pdf-ppt-slides.html>
9. <http://www.authorstream.com/Presentation/ankush85-159135-nphard-nphard171-175-education-ppt-powerpoint/>
10. <http://www.authorstream.com/Presentation/nitinmishra10-83453-complexity-algorithm-data-structure-algorithms-lecture-3-education-ppt-powerpoint/>