GUJARAT TECHNOLOGICAL UNIVERSITY

Master of Engineering Syllabus

Subject Code : 3716306

Subject Name : VLSI Signal Processing

WEF Academic Year :	2023 - 24
Semester :	1
Category of the Course :	Program Elective II

Type of course : Design and analysis of VLSI Signal Processing Systems

Prerequisite : Fundamentals of Digital Electronics and Digital Signal Processing.

Rationale : Studying VLSI Signal Processing offers a unique blend of theoretical knowledge and practical skills, making it an ideal course for students interested in both digital signal processing and VLSI design. By delving this course, students gain a comprehensive understanding of how to develop and implement signal processing algorithms on integrated circuits. This knowledge allows them to bridge the gap between theory and practice, enabling them to design and optimize advanced signal processing systems.

Course Scheme :

Teaching Scheme			Total Credits	Assessment Pattern and Marks				Total Marks
				Theory		Practical		
L	T	PR	C	ESE (E)	PA(M)	ESE (V)	PA (I)	
3	0	2	4	70	30	30	20	150

Course Content :

Sr. No.	Course Content	No. of Hours	% of Weightage
1	**Introduction to DSP algorithms, Iteration bound:** Typical DSP algorithms: Convolution, Correlation, Digital-filters, adaptive filters. Data-flow graph representations, iteration bound and its computation, iteration bound of Multirate data-flow graphs.	10	20
2	**Pipelining, Parallel Processing and Retiming:** Pipelining of FIR filters, Parallel processing, Pipelining and Parallel Processing for low power, definitions and properties of retiming, system inequalities and its solution, retiming techniques.	8	15
3	**Unfolding and Folding:** Algorithm for unfolding, properties of unfolding, Comparative analysis of (i) critical path (ii) unfolding and (iii) retiming. Folding transformation, Register minimization techniques, folding of Multirate systems.	8	15
4	**Systolic Architecture Design:**	6	15

	Systolic array design methodology, FIR systolic arrays, Selection of scheduling vector, Matrix-matrix multiplication and 2D systolic array design, systolic design for space representations containing delays		
5	**Fast Convolution:** Introduction, Cook, Toom Algorithm, Winograd Algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution Algorithm by Inspection.	10	15
	Total	**42**	**100**

Reference Books :

1. Keshab K. Parhi. *VLSI Digital Signal Processing Systems*, Wiley-Inter Sciences, 1999
2. Mohammed Ismail, Terri, Fiez, *Analog VLSI Signal and Information Processing,* McGraw Hill, 1994.
3. Kung. S.Y., H.J. While house T.Kailath, *VLSI and Modern singal processing*, Prentice Hall, 1985.
4. Jose E. France, YannisTsividls, *Design of Analog Digital VLSI Circuits for Telecommunications and Signal Processing*' Prentice Hall, 1994.
5. Magdy A. Bayoumi, E. Swartzlander, "VLSI Signal Processing Technology", Springer Science, 1994.
6. Peter B. Denyer, David Renshaw, "VLSI signal processing: a bit-serial approach", Addison-Wesley, 1985.

Course Outcome :

1. Understanding of VLSI design methodology for signal processing systems.
2. Familiarity with VLSI algorithms and architectures specifically designed for Digital Signal Processing (DSP).
3. Proficiency in implementing basic DSP architectures using Computer-Aided Design (CAD) tools.

Suggested List of Experiments :

1. Compute the iteration bound for the given data flow graph (DFG).
2. Determine the iteration bound for the given multi rate DFG.
3. For given DFG place pipelining register at appropriate places to achieve required sample rate.
4. For given DFG calculate critical path and place pipelining latches to reduce critical paths.
5. For given DFG place pipeline structure to reduce power consumption.
6. Design a given FIR filter with pipeline and parallel processing for power reduction and sampling rate improvement.
7. For given DFG apply retiming techniques to minimize the clock period.
8. Solve the problem of critical path using unfolding techniques for given DFG.
9. Design the folded architecture for the 6-tap FIR filter.

10. Design systolic-architecture for matrix-vector multiplication.
11. Design bit-parallel architecture for six-bit addition.
12. Design a MSD-first radix-4 maximally redundant to non-redundant converter for word length of 8 digits.

List of Open Source Software/learning website :

1. www.nptel.ac.in
2. www.ocw.mit.edu

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