GUJARAT TECHNOLOGICAL UNIVERSITY

Master of Engineering Syllabus

Subject Code : 3716305

Subject Name : VLSI Physical Design

WEF Academic Year :	2023 - 24
Semester :	1
Category of the Course :	Program Elective I

Type of course : Analysis and Design of Floor Planning, Placement and Routing of VLSI Design

Prerequisite : Basic implantation of various Algorithms.

Rationale : The students need to learn basic concepts of VLSI physical design. The students will learn the floor planning and Pin allocations for the VLSI design. The students need to know the basic implementation of Algorithms for the placement and routing. The students will learn the design of various basic of timing analysis and clock tree synthesis.

Course Scheme :

Teaching Scheme			Total Credits	Assessment Pattern and Marks				Total Marks
				Theory		Practical		
L	T	PR	C	ESE (E)	PA(M)	ESE (V)	PA (I)	
3	0	2	4	70	30	30	20	150

Course Content :

Sr. No.	Course Content	No. of Hours	% of Weightage
1	**Introduction to Graph Theory**: Dependency/ Constraint graphs, Steiner Tree, Cliques, Clustering and Spanning Tree	05	10
2	**Circuit Level Partitioning** : Cost function and constrains, Algorithm for Circuit partitioning.	10	20
3	**Floor planning and Pin Allocation :** Floor planning and pin allocation, Problem definition and cost functions.	12	30
4	**Placement and Routing** : Placement and routing Algorithms, cost function and constrains, Area routing, Design Rule Check issue.	08	20
5	**Clock Networks :** Basic concepts in clock networks, modern clock tree synthesis.	02	05
6	**Timing Analysis :** Timing closure, Timing Analysis and Performance constrains, Timing driven placement and routing, Physical synthesis.	05	15
	Total	**42**	**100**

Reference Books :

1. Sadiq M Sait, Habib Youssef, VLSI Physical Design Automation: Theory and Practice Publication: World Scientific.
2. Andrew B Kahng, Jens Lienig VLSI Physical Design: From Graph partitioning to Timing Closure, Publication: Springer.
3. Sung Kyu Lim , Practical Problems in VLSI Physical Design Automation, 2008 edition, Springer.

Course Outcome :

Upon completion of the course, the students will be able to :

1. To design and analyze different concepts of graph theory.
2. To understand basic principle, operation and applications of floor planning and pin allocation.
3. Comprehend and apply various algorithms to circuit partitioning Floor planning, Placement and Routing.
4. To study, analyze and implement the VLSI physical design using CAD tools.

Suggested List of Experiments :

1. Simulation of graph theory for VLSI physical Design using MATLAB.
2. Simulation of Kernighan–Lin (KL) partitioning algorithm using MATLAB.
3. Simulation of Simulated annealing algorithm using MATLAB.
4. Synthesis and simulation of VLSI Design using cadence encounter/Magic/Proton.
5. Perform Floor-planning of VLSI design Cell using ILP solver for Integer Linear Programming.
6. Perform Placement of VLSI design using standard cells.
7. Perform Routing of VLSI design using standard cells.
8. Perform Static Timing Analysis for given logic diagram.
9. Perform zero stack algorithm for given logic diagram.
10. Implement small project on VLSI Physical Design.

List of Open Source Software/ Learning website : https://nptel.ac.in/

Open Source Software: VLSI physical design using CAD tools.

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