GUJARAT TECHNOLOGICAL UNIVERSITY

SUBJECT NAME : Memory Technologies
SUBJECT CODE: 3715412
M.E. (Embedded Systems) SEM-I

Type of course: Program Elective - I

Prerequisite: Digital Circuits, Analog Circuits, VLSI

Rationale: Memory Technology course is essential for understanding variety of memory architecture along with fabrication and testing issues.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks				Total Marks
				Theory Marks		Practical Marks		
L	T	P	C	ESE(E)	PA (M)	PA (V)	PA (I)	
3	0	2	4	70	30	30	20	150

Content:

Sr. No.	Content	Total Hrs	% Weightage
1	**Random Access Memory Technologies:** Static Random Access Memories (SRAMs), SRAM Cell Structures, MOS SRAM Architecture, MOS SRAM Cell and Peripheral Circuit, Bipolar SRAM, Advanced SRAM Architectures, Application Specific SRAMs.	8	15%
2	**Dynamic RAM :** DRAMs, MOS DRAM Cell, BiCMOS DRAM, Error Failures in DRAM, Advanced DRAM Design and Architecture, Application Specific DRAMs.SRAM and DRAM Memory controllers.	8	15%
3	**Non-Volatile Memories:** Masked ROMs, PROMs, Bipolar & CMOS PROM, EEPROMs, Floating Gate EPROM Cell, OTP EPROM, EEPROMs, Non-volatile SRAM, Flash Memories.	8	20%
4	**Semiconductor Memory Reliability and Radiation Effects:** General Reliability Issues, RAM Failure Modes and Mechanism, Nonvolatile Memory, Radiation Effects, SEP, Radiation Hardening Techniques. Process and Design Issues, Radiation Hardened Memory Characteristics, Radiation Hardness Assurance and Testing.	8	15%
5	**Advanced Memory Technologies and High-density Memory Packing Technologies:** Ferroelectric Random Access Memories (FRAMs), Gallium Arsenide (GaAs) FRAMs, Analog Memories, Magneto Resistive Random Access Memories (MRAMs), Experimental Memory Devices.	7	20%
6	**Advancement in Memory Technology** Memory Hybrids (2D & 3D), Memory Stacks, Memory Testing and Reliability Issues, Memory Cards, High Density Memory Packaging	6	15%

Reference Books:

[1] Ashok K Sharma, “Advanced Semiconductor Memories: Architectures, Designs and Applications”, Wiley Interscience
[2] Kiyoo Itoh, “VLSI memory chip design”, Springer International Edition
[3] Ashok K Sharma,” Semiconductor Memories: Technology, Testing and Reliability , PHI

Course Outcomes:

At the end of the course, students will be able to:

- Select architecture and design semiconductor memory circuits and subsystems.
- Identify various fault models, modes and mechanisms in semiconductor memories and testing procedures.
- Knowhow of the state-of-the-art memory chip design

List of Experiments:

1) SPICE Simulation of 6T / 4T cell SRAM cell
2) SPICE Simulation of Bipolar SRAM.
3) SPICE Simulation of DRAM Cell.
4) SPICE Simulation of various sense amplifier circuits
5) SPICE Simulation of address decoding circuit
6) SPICE Simulation of reference voltage generator
7) SPICE Simulation of EEPROM Cell
8) Layout Design and Simulation of SRAM Cell.

Major Equipment:

- SPICE Tool (NGSpice , pSPICE, HSPICE)
- Virtuoso Cadence Tool

List of Open Source Software/learning website:

- NPTEL Lectures