GUJARAT TECHNOLOGICAL UNIVERSITY

RTL SIMULATION AND SYNTHESIS WITH PLDs

SUBJECT CODE: 3710512

ME 1st Semester

Type of course: Major Elective - I

Prerequisite: Digital logic design and any programming language.

Rationale: NA

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks				Total Marks
				Theory Marks		Practical Marks		
L	T	P	C	ESE(E)	PA (M)	PA (V)	PA (I)	
3	0	2	4	70	30	30	20	150

Content:

Sr. No.	Topics	Teaching Hrs.	Module Weightage
1	Top down approach to design, Design of FSMs (Synchronous and asynchronous), Static timinganalysis, Meta-stability, Clock issues, Need and design strategies for multi-clock domain designs.	11	24%
2	Programmable Logic Devices, Introduction to ASIC Design Flow, FPGA, SoC, Floor planning, Placement, Clock tree synthesis, Routing, Physical verification, Power analysis, ESD protection.	12	30%
3	Design for performance, Low power VLSI design techniques. Design for testability.	08	20%
4	IP and Prototyping: IP in various forms: RTL Source code, Encrypted Source code, Soft IP, Netlist, Physical IP, Use of external hard IP during prototyping.	07	17%
5	Case studies and Speed issues.	04	09%
		42	100%

Reference Books:

1. Richard S. Sandige, "Modern Digital Design", MGH, International Editions.
2. Donald D Givone, "Digital principles and Design", TMH
3. Charles Roth, Jr. and Lizy K John, "Digital System Design using VHDL", Cengage Learning.
4. Samir Palnitkar, "Verilog HDL, a guide to digital design and synthesis", Prentice Hall.
5. Doug Amos, Austin Lesea, Rene Richter, "FPGA based prototyping methodology manual", Xilinx
6. Bob Zeidman, "Designing with FPGAs & CPLDs", CMP Books.
7. J. Bhasker, "A VHDL PRIMER, 3/E 3rd Edition

Course Outcome:

At the end of the course, students will demonstrate the ability to:
Familiarity of Finite State Machines, RTL design using reconfigurable logic. Design and develop IP cores and Prototypes with performance guarantees. Use EDA tools like Cadence, Mentor Graphics , Altera and Xilinx.

Suggested List of Experiments:

1. (a) Implement 4 bit adder
   (b) Modify 4 bit adder for carry look ahead concept.
2. Implement 4 bit universal counter with up/down counter, synchronous clear and preset, count enable carry in/out
   facility
3. Implement 4 bit shift register with parallel load, serial in, shift left/right control.
4. Design 4 bit comparator with behavioral and structure architecture.
5. Design 4 bit ALU sequence detector.
6. (a) Design 4X4 bit multiplier
   (b) Design 4X4 booth bit multiplier
7. (a) Design the state machine with combinational output decoding.
   (b) Design the state machine with registered output decoding
   (c) Design the state machine with output encoded within the state bit.
8. Design simple memory controller.
9. Using PSPICE obtain characteristics of MOSFET with resistive load.
10. Using PSPICE obtain characteristics of enhancement MOSFET with resistive load.
11. Using PSPICE obtain characteristics of CMOS.
12. Minimum 2 mini project in the group of two students.

Major Equipments:

Kits with Xilinx / Altera FPGA

List of Open Source Software/learning website:

Xilinx ISE/Altera/cadence