GUJARAT TECHNOLOGICAL UNIVERSITY, AHMEDABAD, GUJARAT

Course Curriculum

DIGITAL MEMORY SYSTEMS (Code: 3331601)

Diploma Programme in which this course is offered	Semester in which offered
Information Technology	3rd Semester

1. RATIONALE

The objective of Digital Memory Systems is to make the students understand the design, types and classification of a digital memory circuit. The recent trend of technology is towards efficient memory structures design and hence it becomes very crucial for the students of diploma in I.T. to understand fundamentals of memory designing and related topics. This Course will enable student to comprehend basic architecture of memory systems including processor architecture and its implementation.

2. COMPETENCIES (Programme Outcomes (POs) according to NBA Terminology):

The course content should be taught and implemented with the aim to develop different types of skills so that students are able to acquire following competencies:

- **Comprehend various digital circuits, their logical functioning and applications.**
- **Illustrate typical architecture of memory and processor.**

3. TEACHING AND EXAMINATION SCHEME

Teaching Scheme (In Hours)			Total Credits (L+T+P)	Examination Scheme				
				Theory Marks		Practical Marks		Total Marks
L	T	P	C	ESE	PA	ESE	PA	150
3	2	2	7	70	30	20	30	

Legends: L - Lecture; **T** - Tutorial/Teacher Guided Student Activity; **P** - Practical; **C** - Credit; **ESE** - End Semester Examination; **PA** - Progressive Assessment

Note: It is the responsibility of the institute heads that marks for **PA of theory & ESE and PA of practical** for each student are entered online into the GTU Portal at the end of each semester within the dates specified by GTU.

4. COURSE DETAILS

Unit	Major Learning Outcomes (Course Outcomes in Cognitive Domain according to NBA terminology)	Topics and Sub-topics
Unit – I Digital Memory Systems Basics	1a.Explain various types of logic gates.	1.1 Logic gates such as AND, OR, NOR, NAND, EX-OR, X-NOR.
	1b. Classify Digital logic families on the basis of various parameters.	1.2 Definition, Classification, Characteristics (Propagation delay, power dissipation, fan-out, fan-in, Noise Margin),comparison between various logic families.(**No circuit design**)
	1c. Design Memory registers for simple applications.	1.3 Flip-flop definition, types and design (R-S , clocked R-S, J-K, D and T)
Unit – II Sequential Circuit Design	2a. Discriminate various types of clock Pulses.	2.1 Definations, requirement and types of clock pulse. (Level triggered and Edge triggered)
	2b. Solve race around problem.	2.2 Issues with J-K Flip-Flop, Master-Slave Flip Flop, Edge Triggered Flip-flop.
	2c. Design sequential circuits for simple applications.	2.3 Excitation table, state table and designing steps of simple sequential circuit design.
Unit – III Complex Sequential Circuit Design	3a.Describe the advanced sequential circuit design.	3.1 4-bit parallel load register design. 3.2 4-bit bi-directional shift register design. 3.3 4-bit binary synchronous counter design. 3.4 4-bit binary(ripple) asynchronous counter design.
Unit – IV Memory Architecture	4a. Describe the various types of memory architecture.	4.1 Memory classification 4.2 Random Access Memory (RAM) (Static and Dynamic RAM) 4.3 Read Only Memory (ROM)(Types, Design of 32 x4 ROM) 4.4 Programmable Logic Array (PLA)(comparison with ROM,simple PLA design) 4.5 Cache(Physical address model, Cache performance, cache addressing)
Unit – V Processor Architecture	5a Classify Flynn's taxonomy .	5.1 Flynn's taxonomy classification.
	5a Explain the various blocks of 8086 processor architecture.	5.2 8086 architecture,Registers,flags,addressing modes, pin diagram) 5.3 Memory segmentation of 8086
	5b Calculate physical and logical address in 8086 processor.	5.4 Physical and logical address calculation

5. SUGGESTED SPECIFICATION TABLE WITH HOURS & MARKS (THEORY)

Unit	Unit Title	Teaching Hours	Distribution of Theory Marks			
			R Level	U Level	A Level	Total Marks
I	Digital Memory System Basics	8	2	4	4	10
II	Sequential circuit design	6	2	4	6	12
III	Complex sequential circuit design	8	4	6	6	16
IV	Memory architecture	10	4	5	6	15
V	Processor architecture	10	4	5	8	17
Total		**42**	**16**	**24**	**30**	**70**

Legends: R = Remember; U = Understand; A = Apply and above levels (Bloom's revised taxonomy)

Note: This specification table shall be treated as only general guideline for students and teachers. The actual distribution of marks in the question paper may slightly vary from above table.

6. SUGGESTED LIST OF EXERCISES/PRACTICAL

The practical/exercises should be properly designed and implemented with an attempt to develop different types of practical skills **(Course Outcomes in psychomotor and affective domain)** so that students are able to acquire the competencies (Programme Outcomes). Following is the list of practical exercises for guidance.

Note: Here only Course Outcomes in psychomotor domain are listed as practical/exercises. However, if these practical/exercises are completed appropriately, they would also lead to development of **Programme Outcomes/Course Outcomes in affective domain** as given in a common list at the beginning of curriculum document for this programme. Faculty should refer to that common list and should ensure that students also acquire those Programme Outcomes/Course Outcomes related to affective domain.

Sr. No.	Unit No.	Practical/Exercise (Course outcomes in Psychomotor Domain according to NBA terminology)	Approx. Hrs. Required
1	I (Any Four)	Simulate basic logic gates using MultiSim/Electronic Work Bench.	2
2		Classify digital logic families.	2
3		Design of NAND logic gate using CMOS logic family.	2
4		Design of NOR logic gate using CMOS logic family.	2
5		Discriminate between flip-flop.	2
6		Design of R-S Flip Flop.	2
7		Design of J-K Flip Flop.	2
8	II (Any Two)	Design of clock pulse generator circuit.	2
9		Simulate clock pulse generator circuit using MultiSim/Electronic Work Bench .	4
10		Develop the excitation table of J-K Flip Flop	2
11		Develop the excitation table of R-S Flip Flop	2
12	III (Any three)	Design of master slave JK Flip Flop.	2
13		Solve simple sequential design problem.	2
14		Solve simple sequential design problem	2
15		Design 4 –bit Register using D- Flip Flop.	2
16		Design 4 –bit Register using T- Flip Flop.	2
17		Design 4 –bit Counter using R-S Flip Flop.	2
18		Design 4 –bit Counter using JK- Flip Flop.	2
19	IV	Design 32x4 ROM	4
20		Design PLA	2
21	V	Identify various blocks of 8086 Architecture	2

7. SUGGESTED LIST OF STUDENT ACTIVITIES

Following is the list of proposed student activities such as:

i. Seminar Presentation
ii. Chart and model Preparation

8. SPECIAL INSTRUCTIONAL STRATEGY (If Any)

i. The subject requires both theory and practical emphasis simultaneously, so that the student can understand the practical significance of the various application areas.
ii. In Unit I & II, III, IV & V the teacher has to play an active role in demonstrating the designing of various sequential circuits and their implementation
iii. The designed circuits available as listed in unit III should be shown to students so they can understand where & how the various circuits are implemented in real application applications.
iv. Students are assigned to prepare various comparative charts for register and counters as mentioned in Unit III.
v. Students should be given enough exposure to variety of simulation software also should be given to students

9. SUGGESTED LEARNING RESOURCES

(A) List of Books:

S. No.	Title of Books	Author	Publication
1	Digital Electronics, 1st Edition	Mandal, Soumitra Kumar	McGraw Hill
2	Digital Electronics, 5th Edition	Green ,D.C.	Pearson Education
3	The x86 microprocessor architecture, programming and interfacing 8086 to Pentium, 1st Edition	Das, Lyla B.	Pearson
4	Advanced computer Architecture, 4th Edition	Kai Hwang	TMH

B. List of Major Equipment/Materials with Major Specifications.

i. Power supply: 10 V.

ii. Digital Trainer kit for flip flops.

iii. Digital Multimeter $3_{1/2}$ digit to measure 5 volt.

iv. CRO with 1 MHz frequency,single trace

v. Clock Pulse Generator for square wave generation of 5 volts.

vi. Components:IC 7400 NAND gate IC, IC 7402 NOR gate IC, IC 7404 NOT gate IC, LED

vii. Consumables:Connecting wires single strained, Patch Chords with banana jack connector with multiple outputs.

C List of Software

i. MultiSIM (Latest version)

ii. Electronic Work Bench (Latest version)

10. COURSE CURRICULUM DEVELOPMENT COMMITTEE

Faculty Members from Polytechnics

- **Prof. Nandu Fatak**, Lecturer IT, Govt. Polytechnic. Ahmedabad
- **Prof. Pooja Garach**, Lecturer IT, Govt. Girls. Polytechnic. Ahmedabad

Coordinator and Faculty Members from NITTTR Bhopal

- **Dr. K. J. Mathai**, Associate Professor Dept. of Computer Engg. and Applications,
- **Dr. R.K. Kapoor**, Associate Professor Dept. of Computer Engg. and Applications,