GUJARAT TECHNOLOGICAL UNIVERSITY, AHMEDABAD, GUJARAT
COURSE CURRICULUM

Course Title: Digital Electronics
(Code: 3322402)

Diploma Programmes in which this course is offered	Semester in which offered
Power Electronics	Second Semester

1. RATIONALE

The aim of introducing this course on digital electronics to impart knowledge of basic building blocks of digital logic circuits. This will enable the student to become aware of various number systems, logic gates and logic families, combinational and sequential logic circuits, which is the foundation for understanding the digital controls, microprocessors and computer systems. Through this course the student will be able to apply the same in almost all areas of electronic control and develop the testing skills.

2. COMPETENCY

The course content should be implemented with the aim to develop different types of skills leading to the achievement of the following competency:

- **Test digital logic circuits.**

3. TEACHING AND EXAMINATION SCHEME

Teaching Scheme (In Hours)			Total Credits (L+T+P)	Examination Scheme				
				Theory Marks		Practical Marks		Total Marks
L	T	P	C	ESE	PA	ESE	PA	
3	2	2	7	70	30	20	30	150

Legends: L-Lecture; **T** – Tutorial/Teacher Guided Theory Practice; **P** - Practical; **C** – Credit **ESE** - End Semester Examination; **PA** - Progressive Assessment

Note: It is the responsibility of the institute heads that marks for **PA of theory** & **ESE and PA of practical** for each student are entered online into the GTU Portal at the end of each semester within the dates specified by GTU.

4. DETAILED COURSE CONTENTS

Unit	Major Learning Outcomes	Topics and Sub-topics
Unit – I **Number System**	1a. Explain different types of numbering systems.	1.1Decimal number, binary number, octal and Hexadecimal number
	1b. Describe weighted and un-weighted codes and their uses.	1.2 Weighted and un-weighted codes BCD, Gray, Excess-3, ASCII, EBCDIC
	1c. Convert decimal to binary, octal, hexadecimal and vice-versa.	1.3 Conversion: Binary, Octal, Decimal and Hexadecimal number systems
	1d. Perform binary arithmetic operations.	1.4Binary addition, subtraction, multiplication, division 1.5 Complements: 1's, 2's, 9's and 10's and its use for subtraction
Unit– II **Logic Gates and Boolean Algebra**	2a.Identify Logic gates.	2.1 Symbol, operation and truth-table: AND, OR, NOT, NAND, NOR, EX-OR, EX-NOR
	2b.Differentiate positive and negative logic system.	2.2 Positive and negative logic system
	2c.Apply laws of Boolean algebra.	2.3 Laws and theorems of Boolean algebra
	2d.Simplify Boolean expressions.	2.4 Boolean expressions :Sum of product and product of sum, Karnaugh maps and its use for simplification up to four variable Boolean expressions, Don't care condition
	2e.Implement the simplified logic circuit.	2.5 The universal building blocks-NAND & NOR, AND-OR network, NAND-NAND networks for implementation of Boolean expressions
Unit – III **Combinational Logic Circuits**	3a. Implement combinational circuits.	3.1 Half adder, full adder, parallel binary adder, 8421 adder, half subtractor , full subtractor, parallel binary subtractor,1's complement subtractor circuit, 2's complement subtractor/adder circuits
	3b.Compare multiplexer and de-multiplexers.	3.2 Encoder, Decoder (2 to 4 line, 3 to 8 line,4 to 16 line), Binary to gray and gray to binary code converters and Comparator, Multiplexers: 2 to1, 4 to1, 8 to1, 16 to1, De-Multiplexers: 1to 2,1to 4,1to 8,1to 16, Parity Generators , parity checkers and their applications
Unit– IV **Sequential Logic Circuits**	4a.Implement sequential circuits and write truth table, excitation table for various Flip Flops.	4.1 S-R flip-flops(FF), edge triggered S-R FF, D FF and edge triggered D FF, JK FF: Edge trigger JK FF, JK master slave FF, Edge Trigger T FF

Unit	Major Learning Outcomes	Topics and Sub-topics
Unit – V **Logic Families**	5a. Compare different bipolar and MOS logic families.	5.1 Classifications of logic families: Saturated and non-saturated logic, RTL, DTL, TTL, MOS & CMOS families. Inverter, Two input NAND & NOR gate 5.2 Two input AND, OR, NAND and NOR gate circuit using DTL logic family, Two input NAND gate circuit using TTL families, Characteristics of TTL family, Three state TTL gates, MOS based NOT gate, Two input NAND & NOR gate, CMOS based NOT gate, Two input NAND & NOR gate

5. SUGGESTED SPECIFICATION TABLE WITH HOURS & MARKS (THEORY)

Unit No.	Unit Title	Teaching Hours	Distribution of Theory Marks			
			R Level	U Level	A Level	Total Marks
I	Number System	07	06	04	02	12
II	Logic Gates and Boolean Algebra	07	06	04	02	12
III	Combinational Logic Circuits	16	08	10	08	26
IV	Sequential Logic Circuits	06	02	04	04	10
V	Logic Families	06	00	04	06	10
	Total	**42**	**22**	**26**	**22**	**70**

Legends: R = Remembrance; U = Understanding; A = Application and above levels (Revised Bloom's taxonomy)

Note: This specification table shall be treated as only general guideline for students and teachers. The actual distribution of marks in the question paper may vary from above table.

6. SUGGESTED LIST OF EXERCISES/PRACTICALS

The experiments should be properly designed and implemented with an attempt to develop different types of skills leading to the achievement of the competency. Following is the list of experiments for guidance.

S. No.	Unit No.	Practical Experiment	Apprx. Hrs. Required
1.	II	Build/Test the basic logic gates (AND, OR and NOT).	02
2.	II	Build/Test the EX-OR, EX-NOR logic gates.	01
3.	II	Build/Test NAND and NOR as universal gate.	02
4.	II	Test the De- Morgan's theorem.	02
5.	III	Build/Test half adder circuit using EX-OR, AND, OR logic gates.	02
6.	III	Build/Test full adder circuit using EX-OR, AND, OR logic gates.	02
7.	III	Build/Test half subtractor circuit using EX-OR, AND, OR logic gates.	02
8.	III	Build/Test full subtractor circuit using EX-OR, AND, OR logic gates.	02
9.	III	Build/Test parallel binary subtractor circuit.	02

S. No.	Unit No.	Practical Experiment	Apprx. Hrs. Required
10.	III	Build/Test 4 bit parallel adder circuit.	02
11.	III	Design 2's compliment adder circuit.	02
12.	III	Design 2's compliment subtractor circuit.	01
13.	III	Build/Test the 2 to 4, 3 to 8, and 4 to 16 lines decoder circuit.	04
14.	III	Design the 4 to 16 lines decoder using 2 to 4 line decoder circuit.	02
15.	III	Build/Test the encoder circuit.	02
16.	III	Build/Test the comparator circuit.	02
17.	III	Build/Test the parity generator, parity checker circuit.	04
18.	III	Build/Test the 2:1, 4:1, 8:1, 16:1 multiplexer circuit.	04
19.	III	Build/Test the 1: 2, 1:4, 1:8, and 1:16 de multiplexer circuit.	04
20.	IV	Build/Test SR flip-flop.	01
21.	IV	Build/Test D flip-flop.	01
22.	IV	Build/Test JK flip-flop.	01
23.	IV	Build/Test JK master slave flip-flop.	02
24.	IV	Build/Test T flip-flop.	01
25.	V	Build/Test basic logic gates using resistors & diodes.	04
		Total	**54**

7. SUGGESTED LIST OF STUDENT ACTIVITIES

i. Student may be asked to collect photographs from internet which is related to field application of various topics.

ii. Teacher guided self-learning activities, course/library/internet/lab based mini-projects etc. These could be individual or group-based.

iii. Student activities like: course/topic based seminars, internet based assignments

Following is the list of suggested tutorial exercises for guidance.

S. No.	Unit No.	Suggested tutorial exercises
1	I	Convert given decimal number to binary, Octal, Hexadecimal number.
2	I	Convert given binary number to decimal, Octal, Hexadecimal number.
3	I	Convert given Octal number to binary, decimal, Octal, Hexadecimal number.
4	I	Convert given Hexadecimal number to binary, decimal, Octal number.
5	I	Convert given binary number to Gray code and Gray code to binary.
6	I	Convert given Decimal number to BCD code and BCD to Decimal number.
7	I	Exercise using format of EXCESS-3 Codes.
8	II	Compare different logic gates and logic families.
9	II	Simplify Boolean Expression using of Boolean laws.
10	II	Implement the simplification techniques using K-Maps.
11	III	Develop various code conversion circuits.
12	IV	Draw symbols, IC's Layout of different flip-flop.
13	V	Draw pin diagram of different TTL different logic gates and logic families.

8. SUGGESTED LEARNING RESOURCES

A. List of Books

S. No.	Title of Book	Author	Publication
1.	Fundamentals of Digital Circuits	A. Anand Kumar	PHI, 2009 or latest
2.	Digital Electronics and Logic Design	Sharma Sanjay	S. K. Kataria & Sons, 2012 or latest
3.	Modern Digital Electronics	Jain R P	TMH, 2009 or latest
4.	Digital Electronics	K. Meena	PHI, 2009 or latest
5.	Digital Electronics Principles	Malvino & Leach	TMH, 2011 or latest
6.	Digital Electronics	Morris Mano	Pearson, 2008 or latest
7.	Digital Fundaments	Floyd Thomas L & Jain	Pearson, 2011 or latest

B. List of Major Equipment/ Instrument

i. Digital Trainer Boards, Logic Probes, Bread board, IC sockets
ii. Multimeter
iii. Cathode ray Oscilloscope
iv. Logic analyzer
v. D.C. Power supply

C. List of Software/Learning Websites

i. Electronic Work Bench/Multi SIM
ii. www.nptl.iitm.ac.in
iii. www.ocw.mit.edu

9. COURSE CURRICULUM DEVELOPMENT COMMITTEE

Faculty Members from Polytechnics

- **Prof.(Smt). J M Patel**, ALPE, Dept. of Power Electronics, Dr. S. & S. S. Ghandhy College of Engg. & Technology, Surat
- **Prof. S A Patel**, LPE, Dept. of Power Electronics, Dr. S. & S. S. Ghandhy College of Engg. & Technology, Surat

Faculty Members from NITTTR Bhopal

- **Prof. (Ms.) Susan S. Mathew**, Associate Professor, Dept. of Electrical & Electronics Engg.
- **Dr. (Ms.) Anjali Potnis**, Assistant Professor, Dept. of Electrical & Electronics Engg.