GUJARAT TECHNOLOGICAL UNIVERSITY

Bachelor/Master of Engineering Syllabus

Subject Code : 3154704

Subject Name : VLSI Technology and Design

WEF Academic Year :	2024-25
Semester :	5
Category of the Course :	Professional/Open Elective

Prerequisite :	**Knowledge of Basic and Digital Electronics**
Rationale :	This course will provide an opportunity to the students to learn about various topics of VLSI such as MOSFET fabrication, its physics, and analysis as well as design of digital circuits using MOSFET device. In laboratory part of this course, students will be given exposure to hardware description language such as VHDL/Verilog for automated design of digital circuits. This subject is very important for the students who would like to pursue their career in VLSI domain.

Course Scheme :

Teaching Scheme			Total Credits	Assessment Pattern and Marks				Total Marks
				Theory		Practical		
L	T	PR	C	ESE (E)	PA(M)	ESE (V)	PA (I)	
3	0	2	4	70	30	30	20	150

Course Content:

Sr. No.	Course Content	No. of Hours	% of Weightage
	Introduction: Overview of VLSI design methodology, VLSI design flow, Design hierarchy, Concept of regularity, Modularity, and Locality, VLSI design style, Design quality, package technology, introduction to FPGA and CPLD, computer aided design technology.	4	9
	MOS Layout Design and Fabrication: Introduction, Fabrication Process flow: Basic steps, C-MOS nWellProcess, Layout Design rules, full custom mask layout design.	5	11
	MOS Transistor: The Metal Oxide Semiconductor (MOS) structure, The MOS System underexternal bias, Structure and Operation of MOS transistor, MOSFET Current-Voltage characteristics, MOSFET scaling and small-geometry effects, MOSFETcapacitances	9	20
	MOS Inverters - Static Characteristics: Introduction, Resistive load Inverter, Inverter with n-type MOSFET load(Enhancement and Depletion type MOSFET load), CMOS Inverter	6	13

	MOS Inverters Switching characteristics and Interconnect Effects: Introduction, Delay-time definitions, Calculation of Delay times, Inverter designwith delay constraints, Estimation of Interconnect Parasitic, Calculation ofinterconnect delay, Switching Power Dissipation of CMOS Inverters	8	18
	Combinational MOS Logic Circuits: Introduction, MOS logic circuits with Depletion nMOS Loads, CMOS logiccircuits, Complex logic circuits, CMOSTransmission Gates (TGs)	5	11
	Sequential MOS Logic Circuits: Introduction, Behavior of Bistable elements, The SR latch circuit, Clockedlatch and Flip-flop circuit, CMOS D-latch and Edge-triggered flip-flop	4	9
	Introduction to ASIC Design Flow and HDLs: ASIC design flow: specification, synthesis, verification, and layout. Introduction to Hardware Description Languages (HDLs): Verilog or VHDL.	4	9
	Total	**45**	**100**

Reference Book:

1. CMOS Digital Integrated circuits – Analysis and Design by Sung – Mo Kang, Yusuf Leblebici, TATA McGraw-Hill Pub. Company Ltd.
2. Basic VLSI Design By Pucknell and Eshraghian, PHI,3rd ed.
3. Introduction to VLSI Systems by Mead C and Conway, Addison Wesley
4. Introduction to VLSI Circuits & Systems – John P. Uyemura
5. Fundamentals of Digital Logic Design with VHDL, Brown and Vranesic
6. FinFETs and Other Multigate Transistors. J. P. Colinge, Springer Publications
7. A Verilog HDL Primer, Bhaskar J.

Course Outcome:

After Completion of the Course, Student will able to:

No	Course Outcomes	RBT Level*
01	Understand the fundamentals of CMOS VLSI and associated technologies.	
02	Solve problems in the design of CMOS logic circuits, with particular reference to speed and power consumption	
03	Understand overall process of VLSI Design flow starting from system level all the way to the transistor level	

*RM: Remember, UN: Understand, AP: Apply, AN: Analyze, EL: Evaluate, CR: Create

Suggested Specification table with Marks (Theory): (For BE only)

Distribution of Theory Marks:
R Level – 20
U Level – 20
A Level – 25
N Level – 15
E Level – 10
C Level - 10

Suggested Course Practical List

1. Introduction to programmable devices (FPGA, CPLD), Hardware Description Language (VHDL), and the use programming tool.
2. Implementation of basic logic gates and its testing.
3. Implementation of adder circuits and its testing.
4. Implementation 4 to 1 multiplexer and its testing.
5. Implementation of 3 to 8 decoder and its testing.
6. Implementation of 8 to 3 priority encoder and its testing.
7. Implementation of J-K and D Flip Flops and its testing.
8. Implementation of sequential adder and its testing.
9. Implementation of BCD counter and its testing.
10. Implementation of two 8-bit multiplier circuit and its testing.
11. Simulation of CMOS Inverter using SPICE for transfer characteristic.
12. Simulation and verification of two input CMOS NOR gate using SPICE.
13. Implementation and simulation of given logic function using dynamic logic.
14. To generate layout for CMOS Inverter circuit and simulate it for verification.
15. To prepare layout for given logic function and verify it with simulations.
16. To measure IDS – VGS and IDS – VDS characteristics of given n-channel and p-channel MOSFETs.
17. To measure propagation delay of a given CMOS Inverter circuit.

List of Laboratory/Learning Resources Required:

Circuit simulator, FPGA/CPLD programming tool, Multimeter, Power supply, function generator, oscilloscope NPTEL, NGspice circuit simulator

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