GUJARAT TECHNOLOGICAL UNIVERSITY

Bachelor of Engineering
Subject Code: 3154107
Semester – V
Subject Name: Computer Architecture

Type of course: Open Elective

Prerequisite: NA

Rationale: Computer Architecture is fundamental course for Robotics and Automation engineers to understand basic structure and operations of a computer. This course is essential for arithmetic, logic unit and cache memories and virtual memories

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks				Total Marks
L	T	P	C	Theory Marks		Practical Marks		
				ESE (E)	PA (M)	ESE (V)	PA (I)	
3	0	0	3	70	30	0	0	100

Content:

Sr. No.	Content	Total Hrs
1	**Basic Structure of a Computer System:-** Functional Units – Basic Operational Concepts – Performance – Instructions: Language of the Computer – Operations, Operands – Instruction representation – Logical operations – decision making – MIPS Addressing.	7
2	**Arithmetic For Computers:-** Addition and Subtraction, Multiplication – Division – Floating Point Representation - Floating Point Operations – Subword Parallelism	6
3	**Processor And Control Unit:-** A Basic MIPS implementation ,Building a Datapath ,Control Implementation Scheme – Pipelining ,Pipelined data path and control ,Handling Data Hazards & Control Hazards , Exceptions.	8
4	**Parallelism:-** Parallel processing challenges – Flynn's classification – SISD, MIMD, SIMD, SPMD, and Vector Architectures - Hardware multithreading – Multi-core processors and other Shared Memory Multiprocessors - Introduction to Graphics Processing Units, Clusters, Warehouse Scale Computers and other Message-Passing Multiprocessors	10
5	**Memory & I/O Systems:-** Memory Hierarchy - memory technologies – cache memory – measuring and improving cache performance – virtual memory, TLB's – Accessing I/O Devices – Interrupts – Direct Memory Access – Bus structure – Bus operation – Arbitration – Interface circuits - USB	8

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Suggested Specification table with Marks (Theory): (For BE only)

Distribution of Theory Marks					
R Level	**U Level**	**A Level**	**N Level**	**E Level**	**C Level**
18%	46%	20%	16%	-	-

Legends: R: Remembrance; U: Understanding; A: Application, N: Analyze and E: Evaluate C: Create and above Levels (Revised Bloom's Taxonomy)

Note: This specification table shall be treated as a general guideline for students and teachers. The actual distribution of marks in the question paper may vary slightly from above table.

Reference Books:

1. David A. Patterson and John L. Hennessy, Computer Organization and Design: The Hardware/Software Interface, Fifth Edition, Morgan Kaufmann / Elsevier, 2014.
2. Carl Hamacher, Zvonko Vranesic, Safwat Zaky and Naraig Manjikian, Computer Organization and Embedded Systems, Sixth Edition, Tata McGraw Hill, 2012.
3. William Stallings, Computer Organization and Architecture – Designing for Performance, Eighth Edition, Pearson Education, 2010.
4. John P. Hayes, Computer Architecture and Organization, Third Edition, Tata McGraw Hill, 2012.
5. John L. Hennessey and David A. Patterson, Computer Architecture – A Quantitative Approach, Morgan Kaufmann / Elsevier Publishers, Fifth Edition, 2012.

Course Outcomes: After learning the course the students should be able to:

Sr. No.	CO statement	Marks % weightage
CO-1	Understand the basics structure of computers, operations and instructions	18%
CO-2	Design arithmetic and logic unit.	16%
CO-3	Understand pipelined execution and design control unit.	20%
CO-4	Understand parallel processing architectures.	26%
CO-5	Understand the various memory systems and I/O communication.	20%

List of Open Source Software/learning website:

- https://nptel.ac.in/courses/106102062/