GUJARAT TECHNOLOGICAL UNIVERSITY

ELECTRONICS & COMMUNICATION (EMBEDDED SYSTEM) (54)

CORTEX-M4 PROCESSOR ARCHITECTURE AND PROGRAMMING

SUBJECT CODE: 2745402

M.E. 4TH SEMESTER

Type of course: Advanced Microprocessor architecture

Prerequisite: Fundamental knowledge of ARM7 processor architecture is required

Rationale:
Enhancement in the ARM processor architecture has resulted in to Cortex-M series architecture. This new architecture retains the best features from the 32-bit ARM architecture with the highly successful Thumb-2 instruction set design whilst adding several new capabilities such as low power consumption, Floating Point Unit, enhanced determinism and improved code density

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks						Total Marks
				Theory Marks		Practical Marks				
L	T	P	C	ESE (E)	PA (M)	ESE (V)		PA (I)		
						ESE	OEP	PA	RP	
3	0	2#	4	70	30	20	10	10	10	150

Content:

Sr. No.	Content	Total Hrs	% Weightage
1	**Background of ARM Processors and ARM Architecture:** Overview of ARM family Processor Evolution, Cortex-M family processor Architecture details with advantages and applications	03	05
2	**Fundamentals of Cortex-M4 architecture:** Registers, Operating Modes, System Control Block, Systick Timer, Nested Vectored Interrupt Controller (NVIC), Exception and Interrupts, Vector Tables, Memory Map, Reset Sequence, Stack Memory Operation, Bus Interface, Memory Protection Unit, Debugging Support	06	15
3	**Instruction Set:** Assembly language basics, Thumb-2 Technology, Instruction set with description for: Moving data, Processing data with Arithmetic and Logic operations, Branch operations, Stack Operations, Pseudo instructions, Instruction Barrier and Memory Barrier Instructions, Saturation Operations, IF-THEN (IT) instructions, Instructions for enhanced DSP operations, Saturated Math operations	06	15
4	**CMSIS Standard and Cortex-M4 Programming:** Introduction to Cortex Microcontroller Software Interface standard (CMSIS), Organization and Standardization of CMSIS Core, CMSIS Core Structure, usage and benefits, CMSIS core register access, Intrinsic instruction, debug functions, Software development flow	08	30
5	**Memory System:** Memory System Features Overview, Memory Maps, Memory	06	15

	endianness, Memory Access Attributes, Default Memory Access Permissions, Bit-Band Operations, Unaligned Transfers, Exclusive Accesses		
6	**Exceptions and Interrupts:** Exception Types, Interrupt Management, Priorities, Exception sequence, NVIC and SCB registers for exception control, Interrupt Masking	**03**	**5**
7	**Low Power and System Control Features:** Low Power Designs, Low power features, Instructions for low power operations	**03**	**5**
8	**Floating Point Operations:** Single and double precision floating point numbers, Floating Point Unit (FPU) overview and registers, Lazy stacking, DSP applications using FPU	**04**	**5**
9	**Debug and Trace Features:** Requirements of Debug and Trace features, Debug Architecture and Interfaces, Debug modes, Data Watchpoint and Trace unit, Instrumentation Macrocell, Embedded Trace Macrocell	**03**	**5**

Reference Books:

1. The Definitive Guide to ARM Cortex-M3 and Cortex M4 Processor by Joseph Yiu, Newness Publication, 3rd Edition
2. The Designer's Guide to the Cortex-M Processor Family, A Tutorial Approach by Trevor Martin, Newness Publication, 1st Edition
3. The insider's Guide to the STM32 ARM based Microcontrollers by Trevor Martin, Hitex Publication, 2nd Edition

Course Outcome:
After learning the course the students should be able:

1. Understanding Cortex – M4 architecture
2. Learn advanced instructions supported in Cortex – M4 architecture
3. Develop programming skills for Cortex – M4 CPU.
4. Application development skill for implementing DSP algorithm with Floating Point Unit

List of Experiments:

1. Introduction to Programming tool chain for Cortex CPU and study CMSIS library functions for Cortex CPU.
2. Write a program to drive GPIO using CMSIS core on STM32F429 Discovery Kit.
3. Write a program to verify Bit Band Memory operations.
4. Write a program to handle touch screen on the Graphic LCD of STM32F429 Discovery board.
5. Write a program to read accelerometer data and display in graphical form on LCD.
6. Write a program to handle an Exception handler using Nested Vector Interrupt Controller.
7. Write a program to implement a System Service Call using SVC instruction.
8. Write a program to handle timer with interrupt for generating PWM wave.
9. Configure Analog to Digital Convertor with Cortex processor to acquire analog signal and store the data in RAM locations.
10. Using Floating point unit, implement FIR filter.

Design based Problems (DP)/Open Ended Problem:

1. In an application requiring multiple keys detection, prepare a keyboard with 4 keys and interface with Cortex CPU. Write a 'c' program to read the key status.

2. Use floating point unit of a Cortex CPU to handle floating point numbers for mathematic operations.
3. Use STM32F429 discovery board to acquire the analog signal and display on graphic LCD with power down mode features.
4. Interface a temperature sensor LM35 with a Cortex CPU and acquire the analog signal and store in memory with the use of DMA controller.
5. Use DMA controller for acquiring audio signal and apply FIR filter for the implementation of Low Pass Filter.
6. Use timer to generate PWM wave as output on port pin that can replace the requirement of Digital to Analog Convertor.

Major Equipment:

i. STM32F429 Discovery Board
ii. Function Generator
iii. Oscilloscope
iv. Digital Multi-meter
v. DC Power Supply (0-30 V)

List of Software:

KEIL MDK 5.0

Learning website:

www.st.com, www.keil.com

Review Presentation (RP): The concerned faculty member shall provide the list of peer reviewed Journals and Tier-I and Tier-II Conferences relating to the subject (or relating to the area of thesis for seminar) to the students in the beginning of the semester. The same list will be uploaded on GTU website during the first two weeks of the start of the semester. Every student or a group of students shall critically study 2 papers, integrate the details and make presentation in the last two weeks of the semester. The GTU marks entry portal will allow entry of marks only after uploading of the best 3 presentations. A unique id number will be generated only after uploading the presentations. Thereafter the entry of marks will be allowed. The best 3 presentations of each college will be uploaded on GTU website.