

# GUJARAT TECHNOLOGICAL UNIVERSITY

## ELECTRONICS & COMMUNICATION (VLSI SYSTEM DESIGN) (42)

### POWER EFFICIENT VLSI DESIGN

**SUBJECT CODE: 2744202**

**M.E. 4<sup>TH</sup> SEMESTER**

**Type of course:** To understand different design techniques for Low Power VLSI Design.

**Prerequisite:** Basics knowledge of CMOS Circuit Design.

**Rationale:** Useful to understand the concepts & techniques of Low Power Circuit Design, to investigate the various source of power dissipation in CMOS Circuit Design.

#### Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks						Total Marks
L	T	P		Theory Marks		Practical Marks				
			ESE (E)	PA (M)	ESE (V)		PA (I)			
		ESE			OEP	PA	RP			
3	2#	0	4	70	30	30	0	10	10	50

#### Content:

Sr. No.	Content	Total Hrs	% Weight age
1	<b>Introduction to Power Efficient VLSI Design</b>	2	6
2	<b>Need for Low Power VLSI Design:</b> Sources of Power dissipation on Digital Integrated circuits. Emerging Low Power Approaches. Physics of Power dissipation in CMOS Devices. Device and Technology Impact on low Power designs.	6	14
3	<b>Dynamic dissipation in CMOS:</b> Transistor sizing and gate oxide thickness, impact of technology Scaling, technology and device innovation.	6	14
4	<b>Power estimation:</b> Simulation Power analysis SPICE circuit simulators, Gate Level Logic simulation, Capacitive power estimation, static state power, gate level capacitance estimation, Architecture level analysis, Data correlation analysis in DSP System. Montecarlo Simulation. Probabilistic Power Analysis: Random Logic Signals, Probability and frequency, Probabilistic Power Analysis techniques, Signal entropy.	6	14
5	<b>Low Power Design:</b> Circuit level: Power consumption in circuits. Flip-flops and latches design, High capacitance nodes, low power digital cells library logic level: Gate reorganization, signal gating, logic encoding, and state machine encoding, pre-computation logic.	6	14
6	<b>Low Power Architecture and Systems:</b> Power and Performance Management, Switching activity reduction, parallel architecture with voltage reduction, flow graph transformation, low power arithmetic components, low power memory design.	6	14
7	<b>Low power Clock Distribution :</b> Power dissipation in clock distribution, single driver Vs distributed buffers, Zero skew Vs tolerable skew, chip and package co design of clock network	5	12

<b>8</b>	<b>Algorithm and architected level methodologies:</b> Introduction, design flow, Algorithm level analysis and optimization, Architectural level estimation and synthesis.	5	12
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### Reference Books:

1. Gray K. Yeap, "Practical Low power Digital VLSI Design", KAP, 2002
2. Rabaey, Pedram, "Low power Design methodologies" Kuwer Academic, 1997
3. Kaushik Roy, Sharat Prasad, "Low Power CMOS VLSI Circuit" Wiley, 2000
4. Kaushik Roy, Kait-SengYo, Low Voltage Low Power VLSI Subsystems, TMH

### Course Outcome:

After learning the course the students should be able to:

1. Understand the need of Power Efficient VLSI Design.
2. Understand the various sources of power dissipation and technology impact on power dissipation.
3. To understand various concept of power estimation techniques.
4. Understand the basic concepts of power efficient circuit design.
5. Understand the various architectural and algorithm level methods and its impact on power dissipation.

### List of Open Source Software/learning website:

Ng-spice

[www.nptel.com](http://www.nptel.com)

[www.nptel.ac.in](http://www.nptel.ac.in)

**Review Presentation (RP):** The concerned faculty member shall provide the list of peer reviewed Journals and Tier-I and Tier-II Conferences relating to the subject (or relating to the area of thesis for seminar) to the students in the beginning of the semester. The same list will be uploaded on GTU website during the first two weeks of the start of the semester. Every student or a group of students shall critically study 2 papers, integrate the details and make presentation in the last two weeks of the semester. The GTU marks entry portal will allow entry of marks only after uploading of the best 3 presentations. A unique id number will be generated only after uploading the presentations. Thereafter the entry of marks will be allowed. The best 3 presentations of each college will be uploaded on GTU website.