GUJARAT TECHNOLOGICAL UNIVERSITY

ELECTRONICS & COMMUNICATION (SIGNAL PROCESSING AND VLSI TECHNOLOGY) (26)

MUTLI GATE TRANSISTORS
SUBJECT CODE: 2742604
SEMESTER: IV

Type of course: Novel Transistor Device Structure

Prerequisite: Sound knowledge of MOSFET device and SCEs

Rationale: The downscaling MOSFET device has reached a physical limit and device performance is suffering from many SCEs such as leakage current, DIBL, velocity saturation, CLM, etc. The multi gate structures are possible solution to address SCEs and to improve device performance. In certain applications, FinFET has already started replacing MOSFET below 32 nm technology. It is very much required that students should be made familiar with FinFET device at post graduate level.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks						Total Marks
L	T	P	C	Theory Marks		Practical Marks				
				ESE (E)	PA (M)	PA (V)		PA (I)		
						ESE	OEP	PA	RP	
4	0	2#	5	70	30	20	10	10	10	150

Content:

Sr. No	Course Content	Hours	% Weightage
1	The SOI MOSFET: from Single Gate to Multigate, MOSFET scaling and Moore’s law, Short-Channel Effects, Gate Geometry and Electrostatic Integrity, History and Multigate MOSFET Physics	**10**	**20**
2	MultiMate MOSFET Technology: Introduction, Active Area: Fins, Gate Stack, Source/Drain Resistance and Capacitance, Mobility and Strain Engineering, Contacts to the Fins	**10**	**20**
3	Physics of the Multigate MOS System: Device electrostatics, Double gate MOS system, Two-dimensional confinement.	**10**	**20**
4	Mobility in Multigate MOSFETs:Introduction, Double-Gate MOSFETs and FinFETs, Silicon multiple-gate nanowires	**12**	**20**
5	Multi-Gate MOSFET Circuit Design: Introduction, Digital Circuit Design, Analog Circuit Design, SOC Design and Technology Aspects	**10**	**20**

References Books:

1. FinFETs and Other Multigate Transistors. J. P. Colinge, Springer Publications
2. Nanoelectronic Circuit Design – Niraj K. Jha and Deming Chen, Springer Publications

Course Outcome:

After learning the course the students should be able to

1. Realize limitations of MOSFET technology.
2. Understand merits of FinFET technology.
3. Study FinFET physics and modeling.
4. FinFET circuit design approaches.
5. Understand various issues with FinFET device.
6. Explore research opportunities in FinFET technology

List of Experiments: Based on above experiment at least 10 experiment

Design based Problems (DP)/Open Ended Problem:

1. Simulate FinFET device for DC characteristics.
2. Measure parameters such SS, DIBL, leakage current and compare the same with corresponding MOSFET technology.
3. Read recent standard publications related to FinFET technology (minimum five) and prepare a report. Presentation can also be arranged at the end of the semester.

Major Equipment/software: FinFET circuit simulator

List of Open Source Software/learning website: NPTEL, NGspice circuit simulator

Review Presentation (RP): The concerned faculty member shall provide the list of peer reviewed Journals and Tier-I and Tier-II Conferences relating to the subject (or relating to the area of thesis for seminar) to the students in the beginning of the semester. The same list will be uploaded on GTU website during the first two weeks of the start of the semester. Every student or a group of students shall critically study 2 papers, integrate the details and make presentation in the last two weeks of the semester. The GTU marks entry portal will allow entry of marks only after uploading of the best 3 presentations. A unique id number will be generated only after uploading the presentations. Thereafter the entry of marks will be allowed. The best 3 presentations of each college will be uploaded on GTU website.