

GUJARAT TECHNOLOGICAL UNIVERSITY

ELECTRONICS & COMMUNICATION (VLSI SYSTEM DESIGN) (42)

HIGH SPEED CMOS VLSI CIRCUIT

SUBJECT CODE: 2734203

M.E. 3rd SEMESTER

Type of course: CMOS Circuit Design.

Prerequisite: Basics knowledge of CMOS Circuit Design

Rationale: High Speed CMOS Design Styles provides a survey of design styles in use in industry, specifically in the high speed microprocessor design community. Logic circuit structures, I/O and interface, clocking, and timing schemes are reviewed and described. Characteristics, sensitivities and idiosyncrasies of each are highlighted.

Teaching and Examination Scheme:

Teaching Scheme			Credits	Examination Marks						Total Marks
L	T	P		Theory Marks		Practical Marks				
			ESE (E)	PA (M)	ESE (V)		PA (I)			
					ESE	OEP	PA	RP		
3	2#	2	5	70	30	20	10	10	10	150

Content:

Sr. No.	Content	Total Hrs	% Weightage
1	Introduction: Impact of scaling on High Speed VLSI Circuit, Inter-Die Variation, Intra-Die Variation, Fail Causes.	6	15
2	Circuit Modelling for High Speed Design: Simple Model: The Elmore's model Complex model: The FAST model, Delay estimation, Power Estimation	10	20
3	Design Styles for High Speed VLSI : Clocked Logic Styles, Non- Clocked Logic Styles, Single-Rail Domino Logic, Dual-Rail Domino Structure, Latched Domino Structure, Clocked Pass gates Logic, Static CMOS.	10	25
4	Latching Strategies: Basic Latch Design, Latching single-ended logic and Differential Logic, Race Free latches for Pre-charged Logic.	8	20
5	Optimization Techniques for High Speed VLSI: Mathematic Optimization, Circuit optimization, CAD tool for optimization.	8	20

Reference Books:

1. Kerry Bernstein & et. al., High Speed CMOS Design Styles, Kluwer, 1999.
2. Ivan Sutherland, Bob Pproull, David Harris, Logical Efforts Designing Fast CMOS Circuits, Kluwer, 1999.
3. Jan M. Rabaey, et all: Digital Integrated Circuit: A Design perspective, second edition, 2003.
4. Design and optimization techniques of high-speed VLSI circuits by Marco Delaurenti, Phd Dissertation, December 1999.

Course Outcome:

After learning the course the students should be able to:

1. Understand the effect of scaling.
2. Understand the different problems related to delay in IC (Integrated Circuit).
3. Learn Circuit modeling for high speed.
4. Understand the different styles for high speed.
5. Learn how the processing speed of the IC is increased.

List of Experiments:

1. To study various EDA tools for high speed CMOS VLSI circuits.
2. To study different circuit modeling techniques for high speed design.
3. To study different optimization techniques for high speed design.
4. To design and simulate of CMOS inverter for high speed application.
5. To design and simulate of CMOS NAND Gate for high speed application.
6. To design and simulate of CMOS NOR Gate for high speed application.
7. To design and simulate of CMOS NAND Gate for high speed application.
8. To design and simulate of CMOS D Latch for high speed application.
9. To design and simulate of CMOS RS Latch for high speed application.
10. To design and simulate of CMOS D FF for high speed application.
11. To design and simulate of CMOS RS FF for high speed application.
12. Case Study

Design based Problems (DP)/Open Ended Problem:

1. To design and simulate of CMOS half adder for high speed application.
2. To design and simulate of CMOS full adder for high speed application.

Major Equipment: Mentor Graphics, TCAD**List of Open Source Software/learning website:**

Ng-spice
www.nptel.com
www.nptel.ac.in

Review Presentation (RP): The concerned faculty member shall provide the list of peer reviewed Journals and Tier-I and Tier-II Conferences relating to the subject (or relating to the area of thesis for seminar) to the students in the beginning of the semester. The same list will be uploaded on GTU website during the first two weeks of the start of the semester. Every student or a group of students shall critically study 2 papers, integrate the details and make presentation in the last two weeks of the semester. The GTU marks entry portal will allow entry of marks only after uploading of the best 3 presentations. A unique id number will be generated only after uploading the presentations. Thereafter the entry of marks will be allowed. The best 3 presentations of each college will be uploaded on GTU website.